

1

2

3

4

Note for customer before using the Altium files

Queries and Notes	Comments
Design files referenced to generate Altium files	AM62L EVM design files on TI.com have been used for converting the Orcad/Allegro design to Altium design files
Use case for the Altium files	We have customer requesting for Altium files and using the .ALG files. The .ALG file is an intermediate converted file
Altium converted files	The Altium converted schematics and PCB files provided has most of the constraints translated and close the Orcad/Allegro design files
Reviews completed	schematic, layout , footprint review
Simulations	The simulations have been performed on Orcad/Allegro design files
List of Altium converted files provided	Refer to Proc180E1-1_Altium_Folders_Files_List document in the download Zip file
Key care about	The required reviews for the converted files have been provided. The boards have not been built and tested. Orcad/Allegro design-based boards have been built and tested.
Recommendations	Customer can use the files to make the required updates. The recommendation is for customer to perform a detailed review to ensure there are no errors before start of board builds

Title		
Size A4	Number PROC181E1-1	Revision
Date:	7-10-2025	Sheet of
File:	D:\Arvind\...\01.SchDoc	Drawn By:

1

2

3

4

AM62L EVM (TMDS62LEVM)

TABLE OF CONTENTS

PAGE	CONTENTS
01	TABLE OF CONTENTS
02	REVISION HISTORY
03	LINKS TO KEY COLLATERALS AND FAQs
04	BLOCK DIAGRAM AM62L EVM
05	BLOCK DIAGRAM XDS110 DEBUGGER
06	POWER ARCHITECTURE BLOCK DIAGRAM
07	POWER SEQUENCE
08	I2C TREE
09	GPIO MAPPING TABLE
10	USB TYPE-C POWER
11	USB TYPE-C POWER CONNECTOR, PRE REGULATOR ENABLE LOGIC AND LEDs
12	PRE-REGULATOR POWER SUPPLY
13	LOW POWER MODE CONFIGURATION - LDO's & RTC SUPPLY SELECTION
14	SOC POWER SUPPLY PMIC - 1 (ALTERNATIVE)
15	SOC POWER SUPPLY PMIC - 2
16	nWAKEUP PUSH BUTTON, LOAD SWITCH AND VPP LDO
17	SOC POWER SUPPLIES, SUPPLY RAILS AND SOC GROUND VSS
18	SOC POWER SUPPLIES - DECAPS
19	SOC WKUP & RTC DOMAIN CLOCK, OSCILLATOR AND CLOCK BUFFER
20	SOC RESET
21	BOOT MODE CONFIGURATION RESISTORS AND DIP SWITCHES
22	SoC DDRSS AND LPDDR4 DEVICE INTERFACE
23	SOC OSPI INTERFACE AND OSPI DEVICE INTERFACE
24	SOC MMC[0:2] INTERFACE AND eMMC FLASH + RESET
25	SD CARD - LOAD SWITCH, LOAD SWITCH RESET LOGIC AND DATA INTERFACE
26	M.2 INTERFACE AND CONNECTOR
27	SOC PERIPHERALS 1 - GPMC AND CPSW3G ETHERNET INTERFACE
28	SOC PERIPHERALS 2 - USB AND DSI INTERFACE

PAGE	CONTENTS
29	SOC PERIPHERALS 3 - McASP, UART, SPI, I2C, MCAN, JTAG, ADC INTERFACE
30	CPSW3G RGMII_1 ETHERNET PHY
31	CPSW3G RGMII_2 ETHERNET PHY
32	POWER SUPPLY (CORE) FOR ETHERNET PHY
33	USB0 TYPE-C DRP
34	USB1 TYPE-A CONNECTOR, VBUS DIVIDER & POWER SWITCH
35	SOC McASP MUX & LEVEL TRANSLATOR 2
36	SOC VOUT0 FET SWITCHES
37	DPI TO HDMI TRANSMITTER INTERFACE
38	AUDIO CODEC
39	SOC MAIN UART1 - FET SWITCH & LEVEL TRANSLATOR 1
40	DSI LCD INTERFACE CONNECTOR AND EXTERNAL MCAN INTERFACE CONNECTOR
41	GPIO EXPANSION CONNECTOR
42	BOOTMODE BUFFERS AND IO EXPANDERS
43	IO EXPANDER & LEDs
44	BOARD ID EEPROM, ADC INTERFACE & TEMPERATURE SENSORS
45	CURRENT MONITORING DEVICES - 1_A
46	CURRENT MONITORING DEVICES - 1_B
47	CURRENT MONITORING DEVICES - 2_A (ALTERNATIVE)
48	CURRENT MONITORING DEVICES - 2_B (ALTERNATIVE)
49	USB TO FT4232 UART BRIDGE
50	FT4232 UART BUFFERS
51	XDS110 DEBUGGER
52	XDS110 JTAG BUFFER
53	XDS110 TEST AUTOMATION BUFFERS
54	JTAG 20 PIN cTI CONNECTOR
55	ASSEMBLY NOTES AND MOUNTING HARDWARE

BOARD REVISION	E1-1
SCHEMATIC VERSION	1.11

D-Note:-

EVM is a processor evaluation board or platform. The EVM is not a reference design. In some cases the EVM implementation may deviate from the optimum solution to provide a better customer experience or provide flexibility for customers to be able to validate the SOC functionality. TI expects and recommends customers to carefully review and follow all requirements defined in the datasheet, silicon errata, and TRM while designing their custom board. The information found in the datasheet should always take precedence over the EVM implementation.

R-Note:-

- * Verify the DNI components configuration with respect to the EVM schematics (Use PDF) after completion of board design before board assembly
- * A standard 5% tolerance resistor can be used for most of the series and parallel pull resistor
- * Be sure to read through all the D-Notes (Design notes), R-Notes (Review notes) and CAD notes during board design and before start of board build.(Refer FAQs listed for additional details)

Title		
Size A4	Number PROC181E1-1	Revision
Date: 7-10-2025	Sheet of	
File: D:\Arvind_102\SchDoc	Drawn By:	

REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.01	8 JAN 2024	Initial Draft derived from AM62P SK - PROC164E1-1 schematics	Mistral Design Team	Nishant	Ajit MB
0.02	11 JAN 2024	Replaced parts : LPDDR4 (2 GB), Updated FT4232 UART section	Mistral Design Team	Nishant	Ajit MB
0.03	12 JAN 2024	Updated power section & PMIC part as per PDN	Mistral Design Team	Nishant	Ajit MB
0.04	16 JAN 2024	Added ADC header, MCAN headers & updated respective net connections	Mistral Design Team	Nishant	Ajit MB
0.05	18 JAN 2024	Updated SoC RTC and SoC Reset section	Mistral Design Team	Nishant	Ajit MB
0.06	19 JAN 2024	- Updated PMIC 1 and PMIC 2 connections - Updated PMIC local caps, GPIO connections & assembly variants	Mistral Design Team	Nishant	Ajit MB
0.07	22 JAN 2024	Implemented Internal review comments and shared to TI for Review	Mistral Design Team	Nishant	Ajit MB
0.08	23 FEB 2024	Implemented Modular approach and shared to TI for the review	Mistral Design Team	Pandiya rajan	Ajit MB
0.09	15 MAR 2024	Updated Block diagrams and ADC header	Mistral Design Team	Pandiya rajan	Ajit MB
0.10	19 MAR 2024	Replaced OSPI NAND flash with new part	Mistral Design Team	Pandiya rajan	Ajit MB
0.11	20 MAY 2024	- Added 0 ohm series resistor to OSPI data lines - Added 2 push buttons for PMIC nWAKEUP logic - Added current monitor for VDDACORE power supply	Mistral Design Team	Pandiya rajan	Ajit MB
0.12	22 MAY 2024	- Added RC circuit for I2C2_SCL and I2C2_SDA - R169, R210, R217 has been DNI'd - Changed Assembly instruction for R215 and R209 to Mount	Mistral Design Team	Pandiya rajan	Ajit MB
0.13	11 JUNE 2024	- Added new connections for No RTC mode in J35 - 5x3 Header - Added GPIO expansion connector - Change PMIC input from VCC_5V0 to VCC_3V3_MAIN	Mistral Design Team	Pandiya rajan	Ajit MB
0.14	02 July 2024	Updated decaps of PMIC 1 and PMIC 2	Mistral Design Team	Pandiya rajan	Ajit MB
0.15	05 July 2024	- Added U81 Buck regulator for 2V5 supply - Removed load switch and added AND gate for the enable logic 3V3 and 5V0 Pre-regulators	Mistral Design Team	Pandiya rajan	Ajit MB
0.16	11 July 2024	- Input power supply of VDD_RTC and VDDS_RTC_1V8 LDO's has been changed to VCC_3V3_MAIN - RTC mode selection header connections has been updated	Mistral Design Team	Pandiya rajan	Ajit MB
0.17	22 July 2024	- PORz (Power ON reset) logic has been changed - Values of Current sense resistors have been changed	Mistral Design Team	Pandiya rajan	Ajit MB
0.18	25 July 2024	Implemented the TI review comments.	Mistral Design Team	Pandiya rajan	Ajit MB
0.19	29 July 2024	- Shunt resistor R3969, R3968 have been placed between J35 and SOC pin - Shunt resistor R3939 has been removed	Mistral Design Team	Pandiya rajan	Ajit MB
0.20	05 AUG 2024	- Changed the value of shunt resistor R426 to 0.02E - Changed the values of shunt resistors R164, R4034 to 0.04E	Mistral Design Team	Pandiya rajan	Ajit MB
0.21	07 AUG 2024	- 1x3 headers (J16, J6, J18) of MCAN have been replaced with 1x4 headers - Changed the package of U47 from 4-Pin X2SON to 5-Pin SOT-23	Mistral Design Team	Pandiya rajan	Ajit MB
0.22	08 AUG 2024	The schematics has been Back annotated	Mistral Design Team	Pandiya rajan	Ajit MB
0.23	20 AUG 2024	- All the D-Notes and CAD Notes have been updated - Block diagrams have been updated	Mistral Design Team	Pandiya rajan	Ajit MB
1.1	18 NOV 2024	- Changed Assembly instruction for R124, C487 & C489 to Mount - C481 value has been changed from 0.1uF to 1uF - R588 & R594 value has been changed from 10K to 1K	Mistral Design Team	Pandiya rajan	Ajit MB
1.2	20 NOV 2024	- The enable logic of Bootmode buffers U111, U114 & U110 have been changed by connecting one of the output of IO Expander to U23 AND gate. - PMIC-2 (U50) and its corresponding inductors and capacitors were mounted as TPS65214x PMIC will be using as primary PMIC for the production build.	Mistral Design Team	Pandiya rajan	Ajit MB
1.3	21 NOV 2024	- PMIC-1 (U48) and its corresponding inductors and capacitors were made as NM J25 and J26 1x2 headers have been added to EXP_PS_3V3_EN and EXP_PS_5V0_EN signals respectively to provide option to select default state of U2 and U4 load switch enable	Mistral Design Team	Pandiya rajan	Ajit MB
1.4	16 Dec 2024	- J27 & J28 1x2 headers have been added to have the option to short the shunt resistor on VDD_RTC (R505) and VDDS_RTC (R516). These two jumpers are DNI'd - SMD TP's are added across the shunt resistor on VDD_RTC (R505) and VDDS_RTC (R516) - For the INA devices, supply has been replaced with VCC_3V3_MAIN instead of VCC_3V3_SYS. - Added level shifter U134 for SoC_I2C1_SDA/SCL between SoC & INA devices for shifting IO level between VCC_3V3_SYS and VCC_3V3_MAIN - J29 (1x2 header) has been added to FET_SELO signal	Mistral Design Team	Pandiya rajan	Ajit MB
1.5	17 Dec 2024	Updated R497 to be mounted with a 0ohm resistor and R154 to be DNI.	Mistral Design Team	Pandiya rajan	Ajit MB
1.6	02 Jan 2025	- All the D-Notes and CAD Notes have been updated - Block diagrams have been updated	Mistral Design Team	Pandiya rajan	Ajit MB
1.7	12 March 2025	The D-Notes and CAD Notes have been updated	Mistral Design Team	Pandiya rajan	Ajit MB
1.8	14 March 2025	- The D-Notes and CAD Notes have been updated - Block diagrams have been updated	Mistral Design Team	Pandiya rajan	Ajit MB
1.9	21 March 2025	- The D-Notes, R-Notes and CAD Notes have been updated - Block diagrams have been updated	Mistral Design Team	Pandiya rajan	Ajit MB
1.10	26 March 2025	Changed part number of AM62L SoC to XAM62L32AOGHAANB	Mistral Design Team	Pandiya rajan	Ajit MB
1.11	01 April 2025	- D-Notes have been updated - Links to key FAQs have been updated	Mistral Design Team	Pandiya rajan	Ajit MB

KEY LINKS TO COLLATERALS

AM62L EVM (TMDS62LEVM): https://www.ti.com/product/AM62L
AM62Lx Sitara™ Processors datasheet : https://www.ti.com/lit/pdf/SPRSPA1
Hardware Design Considerations : https://www.ti.com/lit/pdf/SPRUJC9
DDR Board Design and Layout Guidelines : https://www.ti.com/lit/pdf/sprad06
Schematic Design and Review Checklist for AM62Lx processor family : https://www.ti.com/lit/pdf/SPRADO8
SKs (Starter Kits) for reference : SK-AM62B, SK-AM62B-P1, SK-AM62-LP, SK-AM62-SIP, TMDS62LEVM, SK-AM62A-LP, SK-AM62P-LP

LINKS TO KEY FAQs

https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1478018/faq-am62l-custom-board-hardware-design-collaterals-to-get-started
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1285107/faq-am64x-am243x-am62x-am62ax-am62px-am62d-q1-am62l-custom-board-hardware-design---collaterals-for-reference-during-schematic-design-and-schematics-review
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1478030/faq-am62l-custom-board-hardware-design---faqs-related-to-processor-collaterals-functioning-peripherals-interface-and-evm
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1478025/faq-am62l-custom-board-hardware-design---reusing-ti-evm-design-files
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1318441/faq-am625-am623-am62a-design-recommendations-commonly-observed-errors-during-custom-board-hardware-design-sk-schematics-updates-for-design-update-note
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1478027/faq-am62l-design-recommendations-custom-board-hardware-design--custom-board-schematics-self-review
https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1522815/faq-am62l-am62l32-am62l31-custom-board-hardware-design---available-design-files-and-supported-cad-tools-format-that-can-be-used-during-custom-board-schematic-and-pcb-design

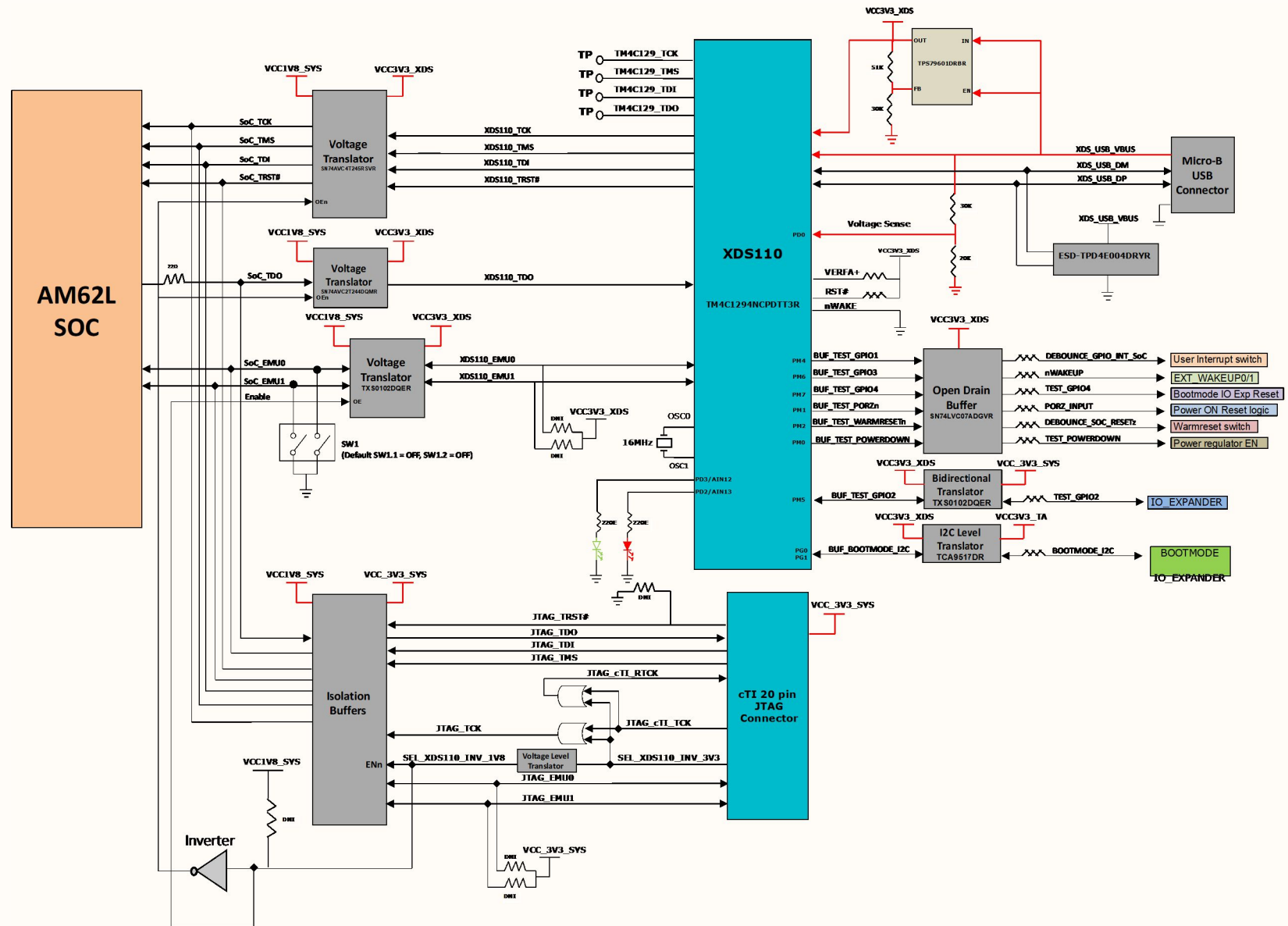
COMMON SOC LVCMOS IO INTERFACE GUIDELINES

1.	Most of the SOC IOs are not fail-safe. No input should be applied before supply ramps.
2.	SOC LVCMOS IOs have slew rate requirements specified, applying a slow ramp input or connecting a cap at the input is not recommended.
3.	Connecting a cap load 50 pF or more at the output is not recommended. DNI cap or perform simulations based on the use case.
4.	SOC IO buffers are off during Reset. A pull is required near to the attached device being driven by the SOC IO that could float.
5.	Any SOC IO that has a trace connected needs a parallel pull. When adding pull is not feasible, ensure the traces are routed away from noisy signals.
6.	Connecting SOC IOs that have alternate function that can be configured directly to supply or ground is not allowed or recommended (including bootmode inputs). (Customer could have bug with their firmware and mis-configure these LVCMOS GPIOs that were intended to be inputs, to be outputs driven logic high instead).
7.	Verify cap loading of the SOC output (when any cap value > 22 pF (use case dependent, max value) is connected, customer needs to simulate), slew rate of the input signal (LVCMOS input slew should be 1000 ns or less), IO compatibility and fail-safe operation between the SOC IOs and attached devices.

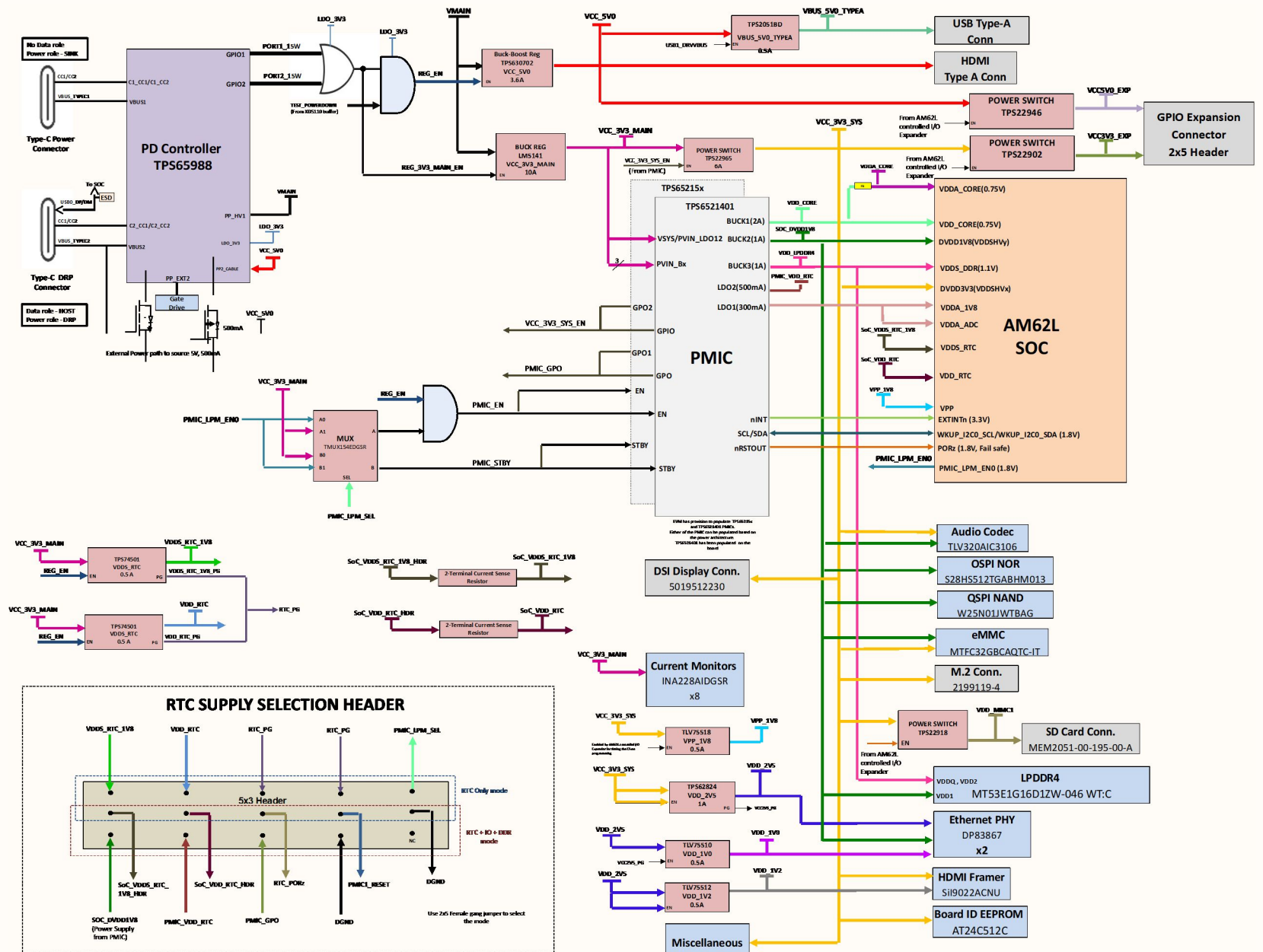
Title		
Size	Number	Revision
A4	PROC181E1-1	
Date:	7-10-2025	Sheet of
File:	D:\Arvind_04\SchDoc	Drawn By:

[illegible]

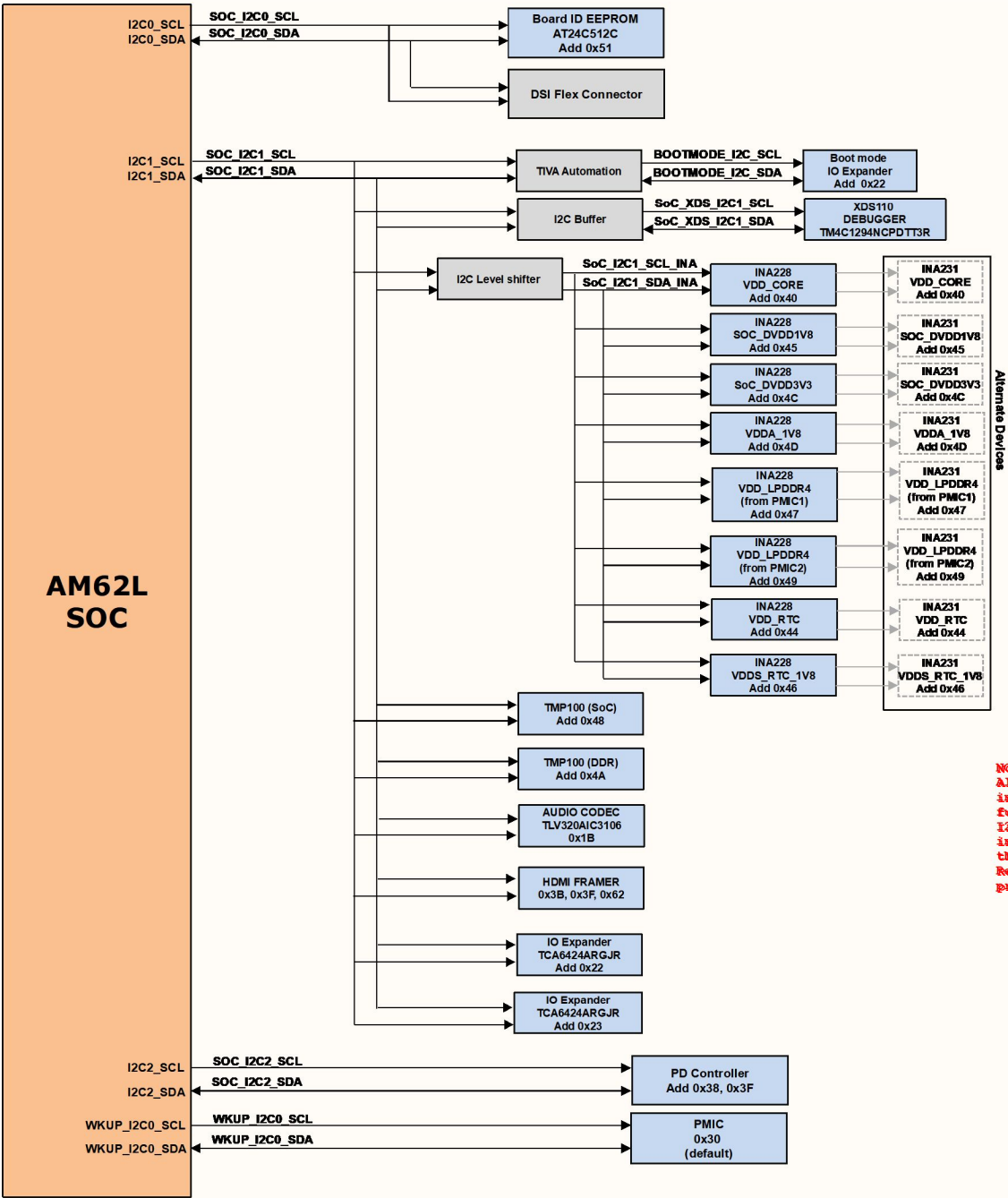
BLOCK DIAGRAM - XDS110 DEBUGGER



POWER ARCHITECTURE BLOCK DIAGRAM



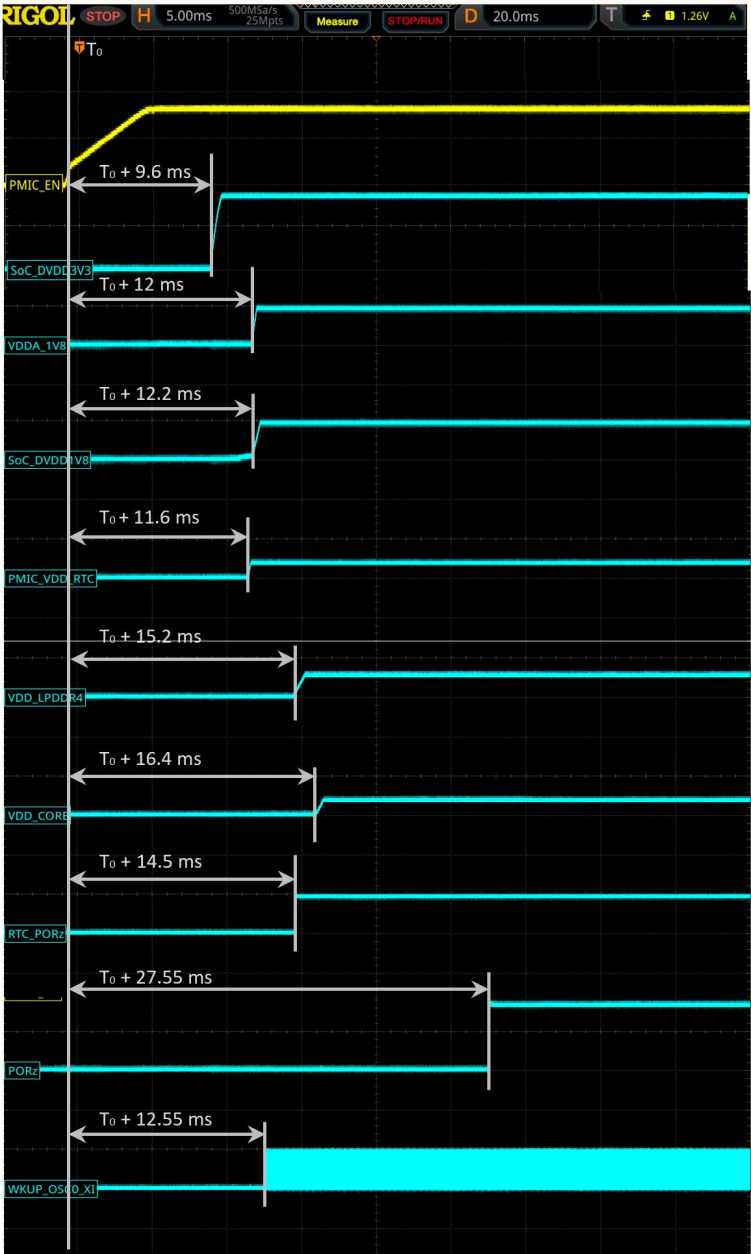
I2C TREE



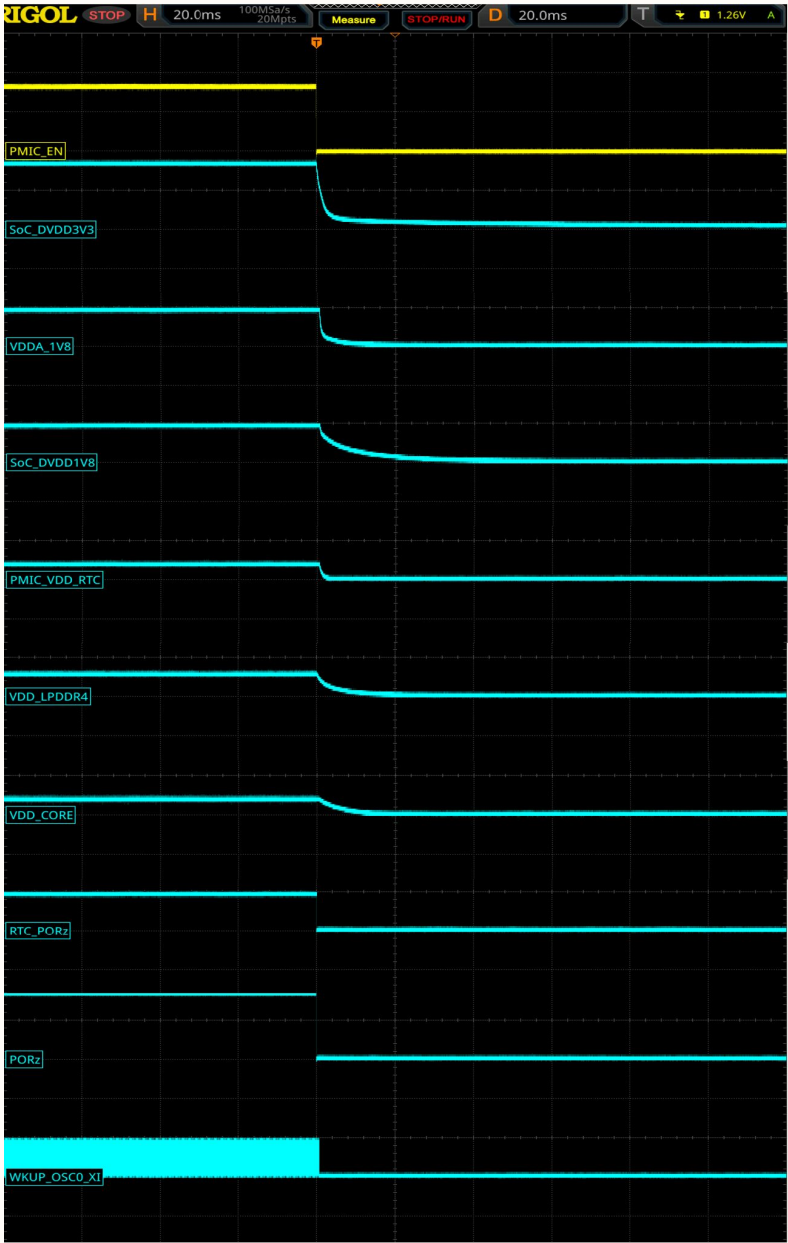
NOTE:
All LVCMOS emulated open drain output type I2C interfaces need a pullup when configured for I2C function.
I2C2 is a open drain output type IO buffer I2C interface. A pullup is recommended irrespective of the IO configuration, when used.
Refer pin connectivity requirements of the processor-specific data sheet.

POWER SEQUENCE - RTC + IO + DDR MODE

POWER-UP SEQUENCE

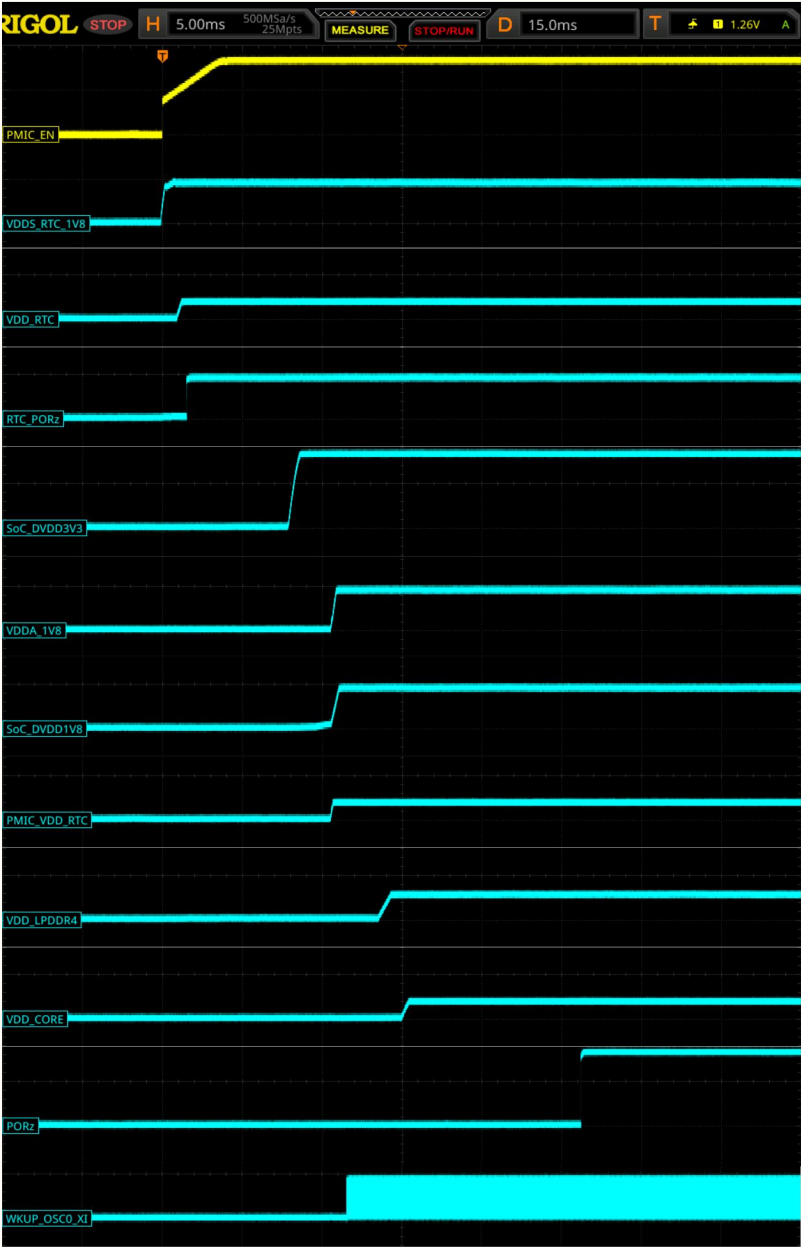


POWER-DOWN SEQUENCE

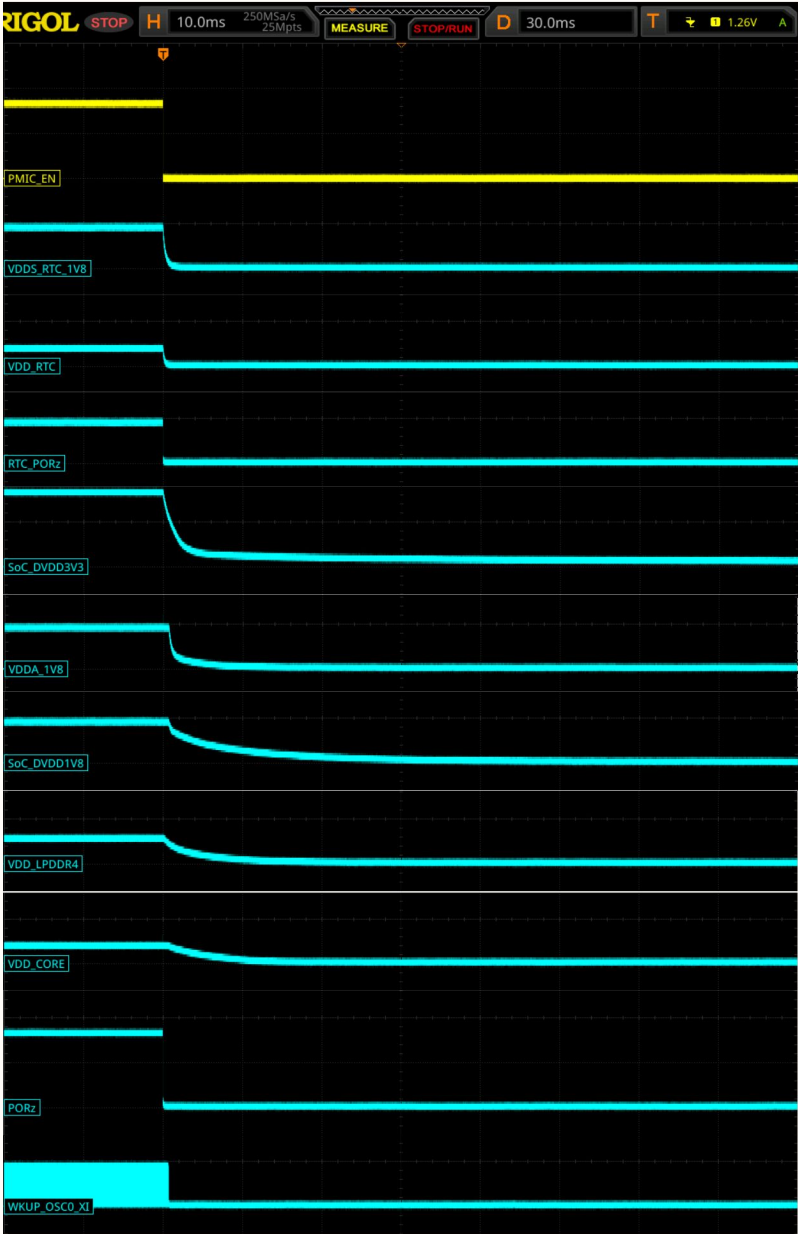


POWER SEQUENCE - RTC ONLY MODE

POWER-UP SEQUENCE



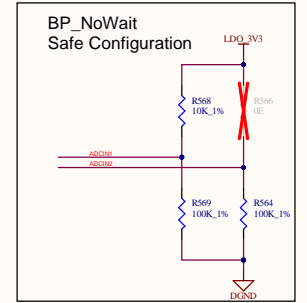
POWER-DOWN SEQUENCE



GPIO MAPPING TABLE

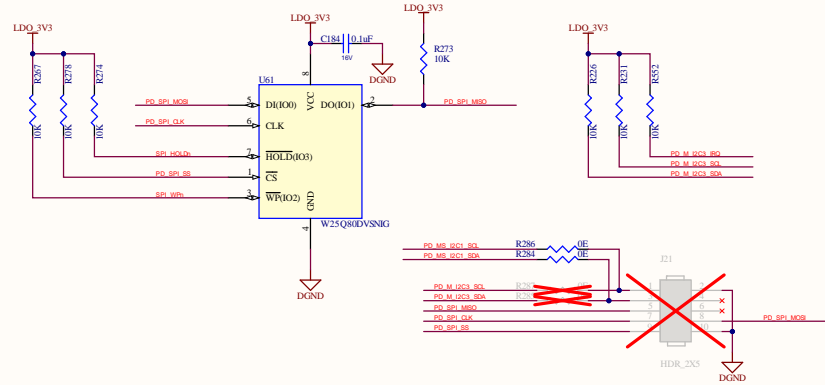
SL NO.	GPIO DESCRIPTION	GPIO NETNAME	FUNCTIONALITY	GPIO USED	PACKAGE SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN ON SOC SIDE	VOLTAGE RAIL CONNECTED ON EVM
1	Enable for WLAN Interface	WLAN_EN	ENABLE	GPIO0_51	MMC2_SD0D	OUTPUT	LOW	HIGH	VDDSHV4	SoC_DVDD1V8
2	WLAN Interrupt	WLAN_IRQ	INTERRUPT	GPIO0_52	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV4	SoC_DVDD1V8
3	OSPI NOR Reset Control GPIO	GPIO_OSPI_NOR_RSTn	RESET	GPIO0_12	OSPI0_Csn1	OUTPUT	HIGH	LOW	VDD0S1	SoC_DVDD1V8
4	OSPI NOR Interrupt	OSPI_NOR_INTn	INTERRUPT	GPIO0_13	OSPI0_Csn2	INPUT	HIGH	LOW	VDD0S1	SoC_DVDD1V8
8	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn	INTERRUPT	GPIO0_105	EXTINTn	INPUT	HIGH	LOW	VDD0SHV1	SoC_DVDD3V3
5	IO Expander Interrupt	GPIO0_91_INTn	INTERRUPT	GPIO0_91	SPID_D1	INPUT	HIGH	LOW	VDD0SHV1	SoC_DVDD3V3
6	User test LED control signal	SOC_GPIO0_123	ENABLE	GPIO0_123	MMC1_SDWP	OUTPUT	LOW	HIGH	VDD0SHV1	SoC_DVDD3V3
7	User Interrupt	GPIO0_90_INTn	INTERRUPT	GPIO0_90	SPID_D0	INPUT	HIGH	LOW	VDD0SHV1	SoC_DVDD3V3
8	PMIC Interrupt	PMIC_nINT	INTERRUPT	GPIO0_105	EXTINTn	INPUT	HIGH	LOW	VDD0SHV1	SoC_DVDD3V3
9	VOUTD FET switch selection	SoC_VOUTD_FET_SEL1	SELECTION	GPIO0_87	SPID_CS0	OUTPUT	HIGH	NA	VDD0SHV1	SoC_DVDD3V3
10	VOUTD FET switch selection	SoC_VOUTD_FET_SEL0	SELECTION	GPIO0_89	SPID_CLK	OUTPUT	HIGH	NA	VDD0SHV1	SoC_DVDD3V3
IO EXPANDER – 01										
1	UART1 FET selection control	UART1_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P02		OUTPUT	HIGH	NA		VCC_3V3_S1S
2	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER-P03		OUTPUT	HIGH	HIGH		VCC_3V3_S1S
3	SOC eFuse Voltage(VPP~1.8V) Regulator Enable	VPP_LDO_EN	ENABLE	IO EXPANDER-P04		OUTPUT	LOW	HIGH		VCC_3V3_S1S
4	EXP CONN 3.3V Power Switch Enable	EXP_PS_3V3_EN	ENABLE	IO EXPANDER-P05		OUTPUT	LOW	HIGH		VCC_3V3_S1S
5	SOC UART1 Mux Enable	UART1_FET_BUF_EN	ENABLE	IO EXPANDER-P06		OUTPUT	HIGH	LOW		VCC_3V3_S1S
6	DSI Display GPIO0	DSI_GPIO0	GPIO	IO EXPANDER-P10		BIDIRECTIONAL	NA	NA		VCC_3V3_S1S
7	DSI Display GPIO1	DSI_GPIO1	GPIO	IO EXPANDER-P11		BIDIRECTIONAL	NA	NA		VCC_3V3_S1S
8	BT UART WAKEUP Signal	BT_UART_WAKE_SOC_3V3	INTERRUPT	IO EXPANDER-P13		INPUT	HIGH	LOW		VCC_3V3_S1S
9	USB Type A overcurrent Indicator	USB_TYPEA_OC_INDICATION	INTERRUPT	IO EXPANDER-P14		INPUT	HIGH	LOW		VCC_3V3_S1S
10	WLAN Alert Interrupt	WLAN_ALERTn	INTERRUPT	IO EXPANDER-P17		INPUT	HIGH	LOW		VCC_3V3_S1S
11	HDMI Interrupt	HDMI_INTn	INTERRUPT	IO EXPANDER-P20		INPUT	HIGH	LOW		VCC_3V3_S1S
12	TEST GPIO2	TEST_GPIO2	GPIO	IO EXPANDER-P21		NA	HIGH	NA		VCC_3V3_S1S
13	MCASPD Enable and Direction Control	MCASPD_FET_EN	ENABLE	IO EXPANDER-P22		OUTPUT	LOW	LOW		VCC_3V3_S1S
14		MCASPD_BUF_BT_EN	ENABLE	IO EXPANDER-P23		OUTPUT	LOW	HIGH		VCC_3V3_S1S
15		MCASPD_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P24		OUTPUT	HIGH	NA		VCC_3V3_S1S
16	DSI to HDMI Card Device ID Interrupt	DSI_EDID	INTERRUPT	IO EXPANDER-P25		INPUT	HIGH	LOW		VCC_3V3_S1S
17	Power Delivery I2C Interrupt Request	PD_I2C_IRQ	INTERRUPT	IO EXPANDER-P26		INPUT	HIGH	LOW		VCC_3V3_S1S
18	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER-P27		OUTPUT	LOW	HIGH		VCC_3V3_S1S
IO EXPANDER – 02										
1	M.2 module Bluetooth LDO Enable	BT_EN_SOC	ENABLE	IO EXPANDER-P00		OUTPUT	HIGH	HIGH		VCC_3V3_S1S
2	VOUTD FET switch selection	VOUTD_FET_SEL0	SELECTION	IO EXPANDER-P01		OUTPUT	LOW	NA		VCC_3V3_S1S
3	M.2 Interface Level Translator Enable	WL_IT_EN	ENABLE	IO EXPANDER-P10		OUTPUT	HIGH	HIGH		VCC_3V3_S1S
4	EXP CONN 5V Power Switch Enable	EXP_PS_5V0_EN	ENABLE	IO EXPANDER-P11		OUTPUT	LOW	HIGH		VCC_3V3_S1S
5	QSPI NAND Reset Control GPIO	GPIO_QSPI_NAND_RSTn	RESET	IO EXPANDER-P20		OUTPUT	HIGH	LOW		VCC_3V3_S1S
6	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTn	RESET	IO EXPANDER-P21		OUTPUT	HIGH	LOW		VCC_3V3_S1S
7	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER-P22		OUTPUT	HIGH	LOW		VCC_3V3_S1S
8	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER-P23		OUTPUT	HIGH	LOW		VCC_3V3_S1S
9	Bootmode Buffer Enable	GPIO_BOOTMODE_BUF_ENz	ENABLE	IO EXPANDER-P24		OUTPUT	HIGH	LOW		VCC_3V3_S1S
10	Audio Codec Reset Control GPIO	GPIO_AUD_RSTn	RESET	IO EXPANDER-P25		OUTPUT	HIGH	LOW		VCC_3V3_S1S
11	eMMC Reset control GPIO	GPIO_EMMC_RSTn	RESET	IO EXPANDER-P26		OUTPUT	HIGH	LOW		VCC_3V3_S1S
12	WLAN Reset control GPIO	SOC_WLAN_SDIO_RST	RESET	IO EXPANDER-P27		OUTPUT	HIGH	LOW		VCC_3V3_S1S

TYPE-C DUAL PD CONTROLLER

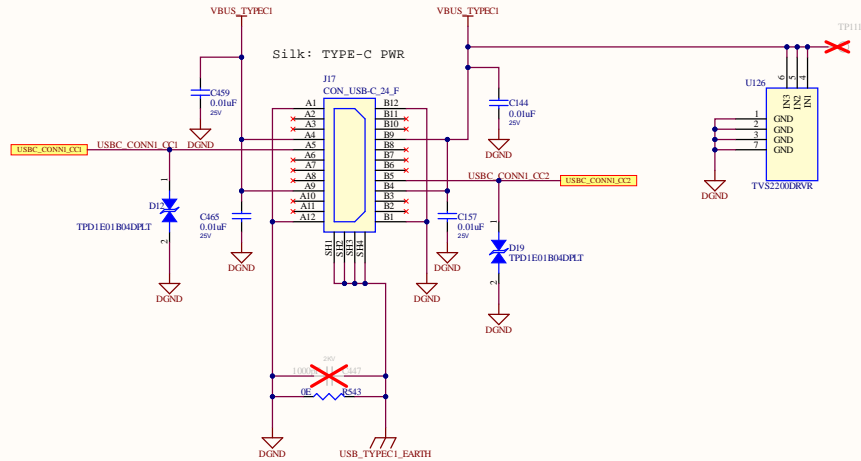


I2C Slave Address	Port1	Port2
I2C2(Default)	0x38	0x3F
I2C1	0x20	0x24

W25Q80DVSNIC

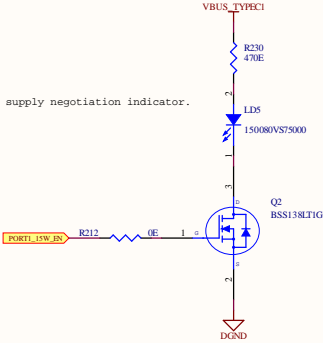


USB TYPE-C POWER CONNECTOR



PORT1_15W_EN STATUS INDICATION LED

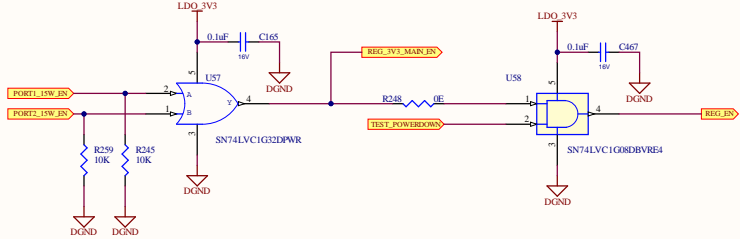
R-Note :-
The LED state is the supply negotiation indicator.
ON indicates success.



POWER INDICATION LED: VBUS_TYPEC1



PRE REGULATOR POWER SUPPLY ENABLE LOGIC

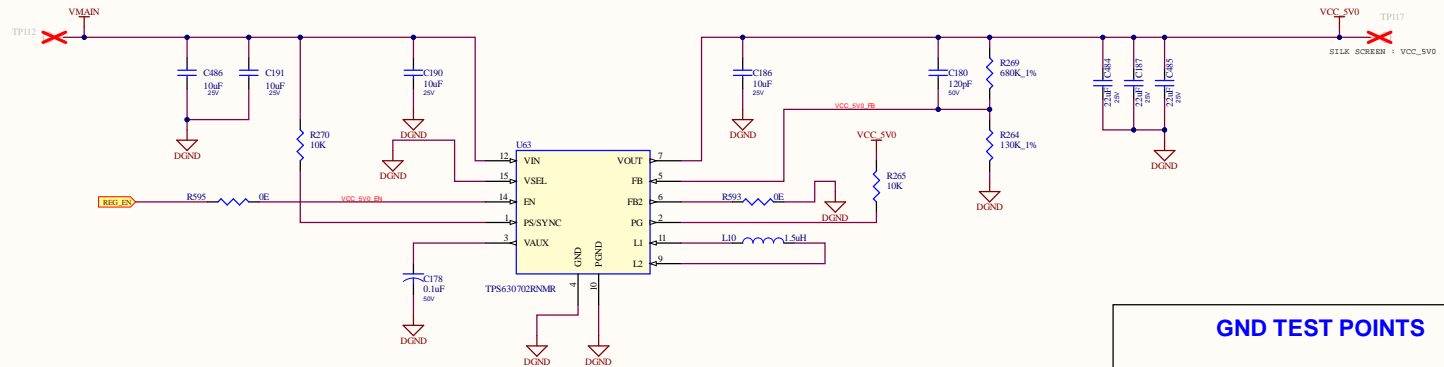


D-Note :-
REG_3V3_MAIN_EN is enabled only when
a 15w or above pd negotiation succeeds.
On custom board designs, ORing logic can
be removed when USB PD controller is not used.

D-Note :-
The TEST_POWERDOWN is by default HIGH
and is used to turn-OFF the PMIC, U63,
U107, U113 through on-board XDS110.
For custom designs, the ANDing logic can be
removed when on-board XDS110 is not used.

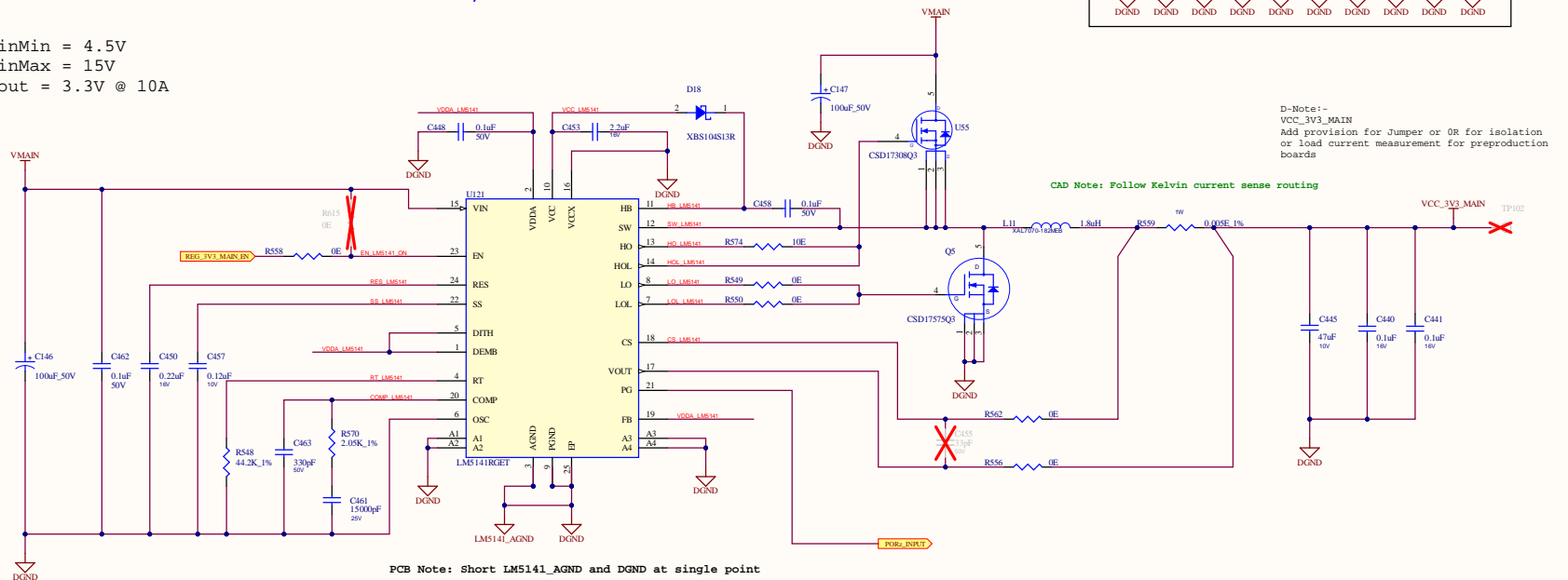
Title			Revision
Size	Number		
A4	PROC181E1-1		
Date:	7-10-2025	Sheet of	
File:	D:\Arvind_113\SchDoc	Drawn By:	

```
VinMin = 4.5V
VinMax = 15V
Vout = 5V @ 2A
```



3.3V, 10.0 AMPS SUPPLY

```
VinMin = 4.5V
VinMax = 15V
Vout = 3.3V @ 10A
```



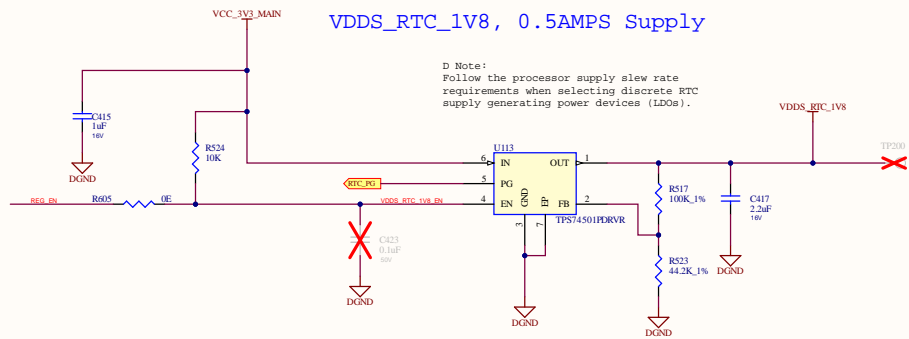
D-Note:-
VCC_3V3_MAIN
Add provision for Jumper or OR for isolation
or load current measurement for preproduction
boards

CAD Note: Follow Kelvin current sense routing

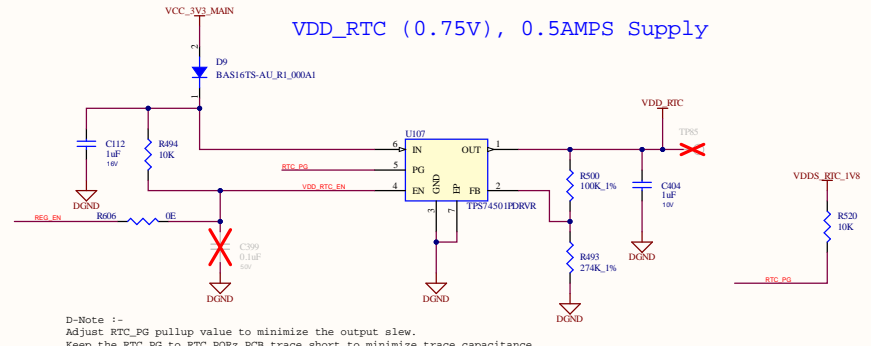
PCB Note: Short LM5141_AGND and DGND at single point

Title		
Size A4	Number PROC181E-1	Revision
Date: 7-10-2025	Sheet of	
File: D:\Arvind\...14.SchDoc	Drawn By:	

LOW POWER MODE CONFIGURATION

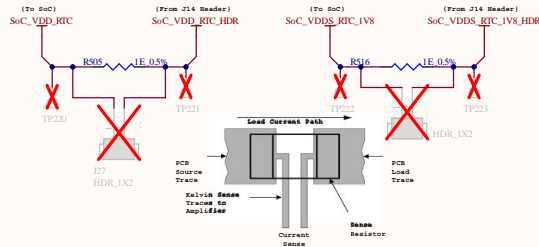


D-Note :-
The enable pin of the discrete RTC supply (LDO) can be driven by the power-good signal of the regulator generating the main supply rail (VCC_3V3_MAIN).
In case the regulator does not support a PG signal- output, a resistor pulled up to the LDO supply input can be used as EN input.



D-Note :-
Adjust RTC_PG pullup value to minimize the output slew.
Keep the RTC_PG to RTC_PORz PCB trace short to minimize trace capacitance.
Adjust the value of the external pullup resistor when an open-drain output PG is used as reset input to RTC_PORz.
The RTC_PORz input has internal hysteresis and the internal reset could glitch when a slow rising input is applied.
The slew rate is recommended to be faster than the limits specified in the LVCMOS IO buffer electrical specification to minimize possible noise coupling.

CURRENT SENSE RESISTOR FOR SoC_VDD_RTC AND SoC_VDDDS_RTC_1V8



CAD NOTE:-
Follow Kelvin current sense routing for RTC supplies current sense resistor (R505 and R516). Follow the routing shown in the above figure that has been added as reference for kelvin current sense routing.

RTC SUPPLY SELECTION

Note : Notes on SoC_VDD_RTC and SoC_VDDDS_RTC_1V8 supply source:

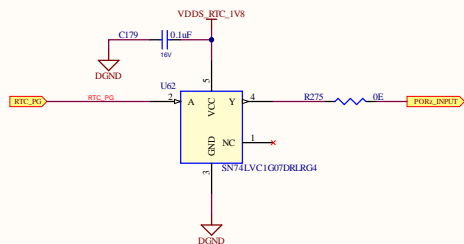
RTC ONLY MODE - external discrete LDOs U113 (for SoC_VDDDS_RTC_1V8) and U107 (for SoC_VDD_RTC) are used.

RTC + IO + DDR MODE - PMIC Buck2 (for SoC_VDDDS_RTC_1V8) and LD01 (in case of PMIC1 - TP865215 is used)/ LD02 (in case of PMIC2 - TP865214 is used) (for SoC_VDD_RTC) are used.

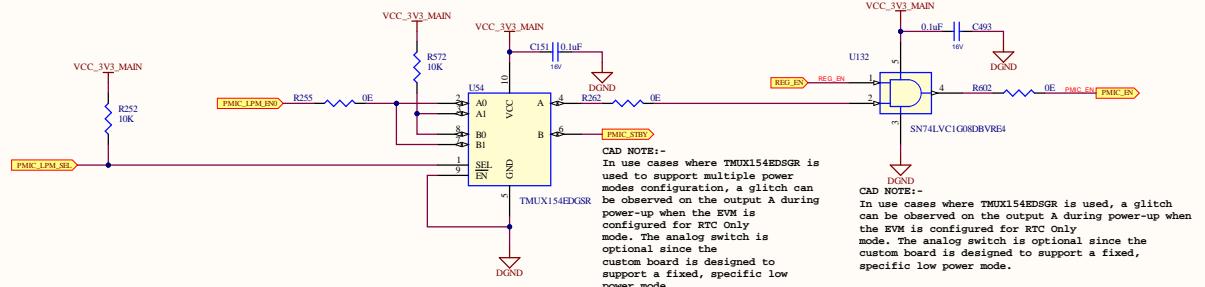
RTC Only MODE	TO SOC	RTC + IO + DDR MODE
VDDDS_RTC_1V8	SoC_VDDDS_RTC_1V8	SOC_DVDD1V8
VDD_RTC	SoC_VDD_RTC	PMIC_VDD_RTC
RTC_PG	RTC_PORz	PMIC_GPO
RTC_PG	PMIC1_RESET (To PMIC 1)	DGND
DGND	PMIC_LPM_SEL	NC

Note: Use 5x2 Female gang jumper to select the mode

RTC_PG TO PORz_INPUT OPEN DRAIN BUFFER



LOW POWER MODE TRIGGER SELECTION



CAD NOTE:-
PMIC_LPM_SEL is generated based on 5x2 Female gang jumper configuration.
By default the MUX_SEL pin is high and PMIC_LPM_ENO drives the PMIC STBY pin to turn-OFF the CORE and VDDA to support RTC + IO +DDR Mode.
When the MUX_SEL pin is low, the PMIC_LPM_ENO drives the PMIC enable pin to support "RTC only". In this low power mode, the entire PMIC is turned-OFF and the RTC domain is supplied by external always-ON LDOs.

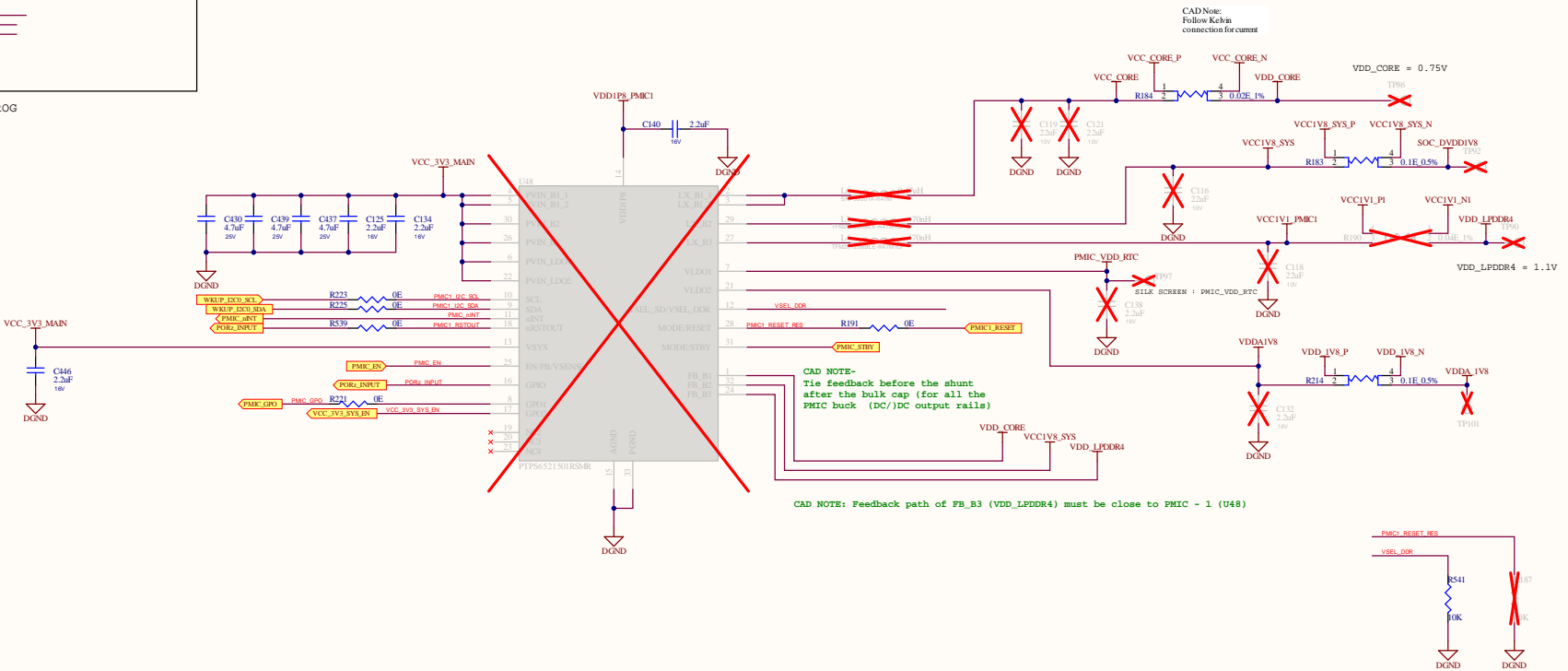
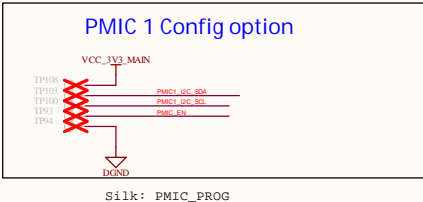
CAD NOTE:-
In use cases where TMUX154EDSGR is used to support multiple power modes configuration, a glitch can be observed on the output A during power-up when the EVM is configured for RTC Only mode. The analog switch is optional since the custom board is designed to support a fixed, specific low power mode.

CAD NOTE:-
In use cases where TMUX154EDSGR is used, a glitch can be observed on the output A during power-up when the EVM is configured for RTC Only mode. The analog switch is optional since the custom board is designed to support a fixed, specific low power mode.

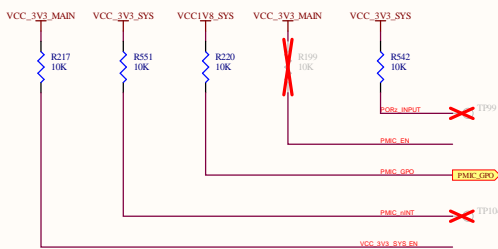
nEN	SEL	OUTPUT & MODE
L	L	A=A0 B=B0 RTC ONLY MODE
L	H (DEFAULT)	A=A1 B=B1 RTC + IO + DDR MODE

Title	
Size A4	Number PROC181E1-1
Date 7-10-2025	Revision 1
File D:\Arvind\J15&HDoc	Sheet of 1
Drawn By:	

SOC POWER SUPPLY PMIC - 1



COMMON PULL-UPS OF PMIC - 1 AND PMIC - 2



D-Node i-
PORZ_INPUT

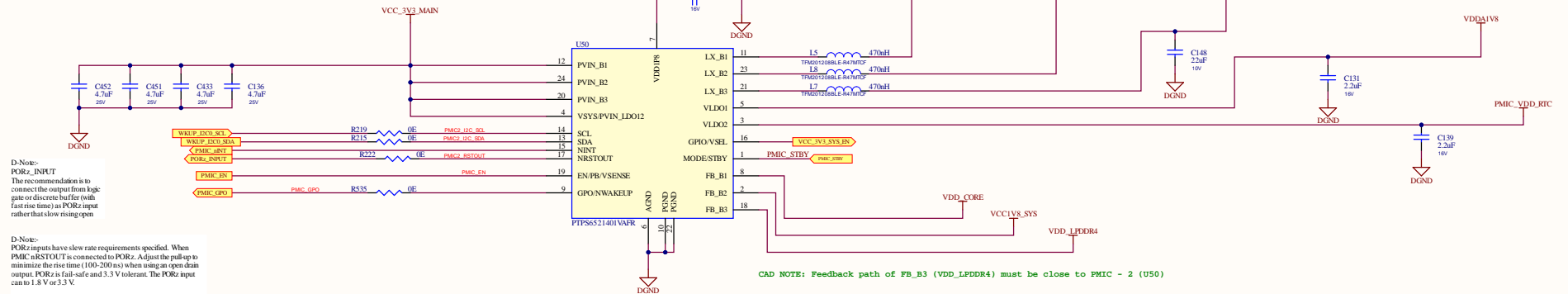
When nRSTOUT from the PMIC is connected directly to PORZ input, adjust nRSTOUT pullup value to minimize the PORZ trace slow rise time to meet the hysteresis and the external pullup value when using an open-drain output to meet the processor slow requirement. The slew rate is recommended to be faster than the limit specified in the IO buffer electrical specification to minimize possible noise coupling. The recommendation is to connect nRSTOUT through a Schmitt trigger push pull output buffer to the PORZ input of the processor. The PORZ input has internal hysteresis and the internal reset could glitch when a slow rising input is applied.

Title			
Size A4	Number PROC181E1-1		Revision
Date:	7-10-2025	Sheet of	
File:	D:\Arvind\16 SchDoc	Drawn By:	

SOC POWER SUPPLY PMIC - 2

PMIC 2 Config option

TP56 ~~PMIC2_LDO_B0A~~
TP58 ~~PMIC2_LDO_B0A~~



The nWAKEUP push button is connected to the EVM for testing. The recommendation is to connect the processor EXT_WAKEUP pin through a Schmitt trigger buffer (Refer RESET & INITIALIZATION custom board).

1.8V VPP (eFUSE), 0.5AMPS SUPPLY

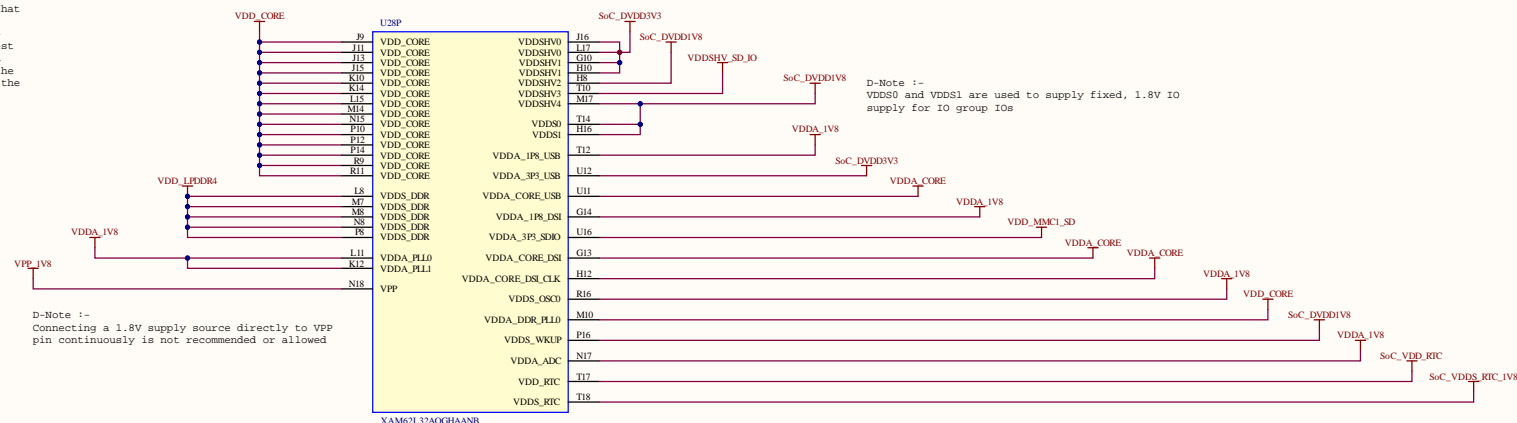
Title		
Size A4	Number PROC181E1-1	Revision
Date: 7-10-2025	Sheet of	
File: D:\Arvind\...18.SchDoc	Drawn By:	

SOC POWER SUPPLIES AND SUPPLY RAILS

D-Note :-

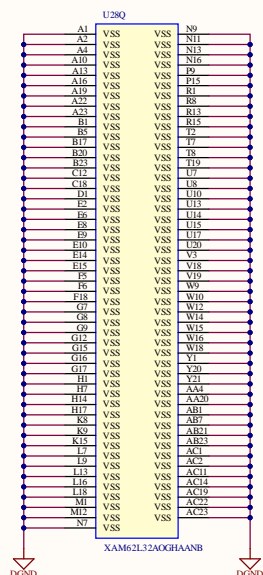
A Trace connected to SOC pad (IO) is effectively an antenna that can pick up noise.

A potential will be generated on the trace when noise couples into the antenna. This potential will be largest on the highest impedance end of the trace. By placing a pull-up or pull-down near the SoC pin (input), we force the highest potential to the open-circuit end of the signal rather than the SoC IO end of the

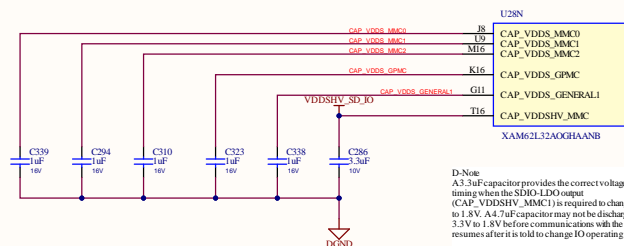


D-Note :-
Refer pin connectivity table of the SOC data sheet for connecting the USB IO, analog and core supplies when USB interface is not used. It is acceptable to have the supplies connected and all the USB pins left unconnected provided the USB driver is not initialized any time and the USB calibration procedure does not happen. Grounding the USB supplies as per pin connectivity requirements when not used saves power when low power is a critical requirement.

SOC VSS



- D-Note :-
 - Common SOC LVCMOS IO interface guidelines
 - 1. Most of the SOC IOs are not fail-safe. No input should be applied before SOC supplies ramp up.
 - 2. SOC LVCMOS inputs have minimum slew rate requirements specified
 - 3. SOC IO buffers are off during Reset and after Reset. A pull is required in the absence of or the attached device inputs could float.
 - 4. Any SOC IO that has a trace connected and not being actively driven needs a parallel pull.
 - 5. When adding pull is not feasible, ensure the traces are routed away from noisy signals

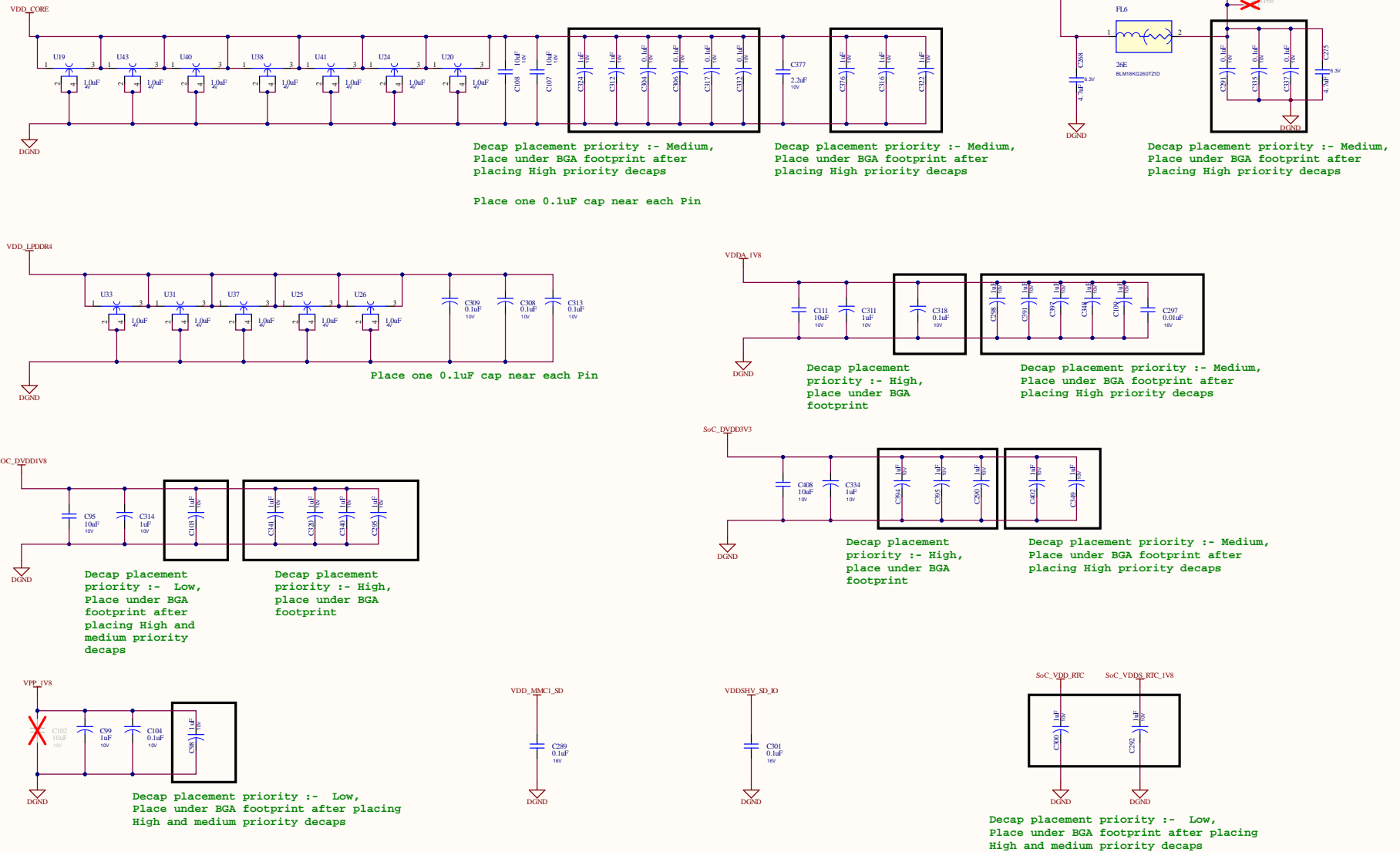


D-Note :-
Select capacitor with ESR < 1 ohm
Ensure the PCB loop inductance is < 2.5 nH
Select 0201 package or smallest possible package nearest to 0201
Refer SOC Data sheet

D-Note
A3.3uF capacitor provides the correct voltage transition timing when the SDIO-LDO output (CAP_VDDSHV_MMC1) is required to change from 3.3V to 1.8V. A4.7uF capacitor may not be discharged from 3.3V to 1.8V before communications with the SD card resumes after it is told to change IO operating voltage.

Title		
Size A4	Number PROC181E-1	Revision
Date: File:	7-10-2025 D:\Arvind\...19 SchDoc	Sheet of Drawn By:

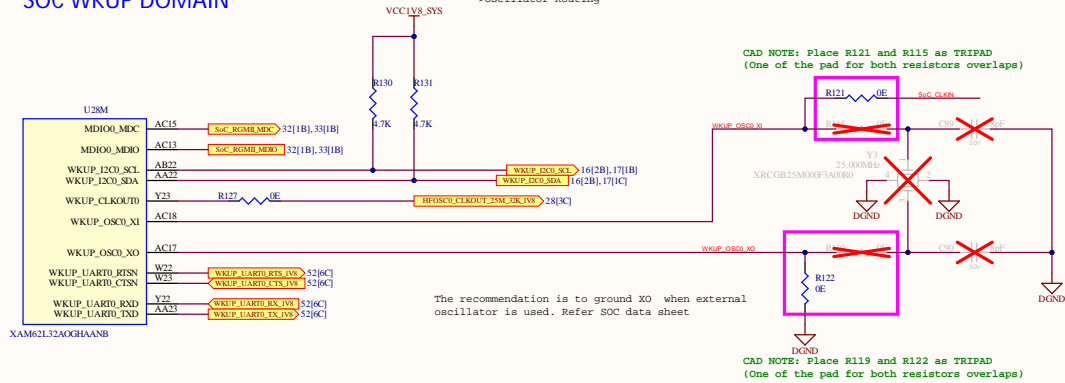
SOC POWER SUPPLIES - DECAPS



R-Note :-
Use of 3 terminal caps optimizes use of
bulk caps quantity and minimizes the PCB loop inductance.

Title		
Size A4	Number PROC181E1-1	Revision
Date 7-10-2025	Sheet of	
File D:\Arvind\2025\Doc	Drawn By:	

SOC WKUP DOMAIN

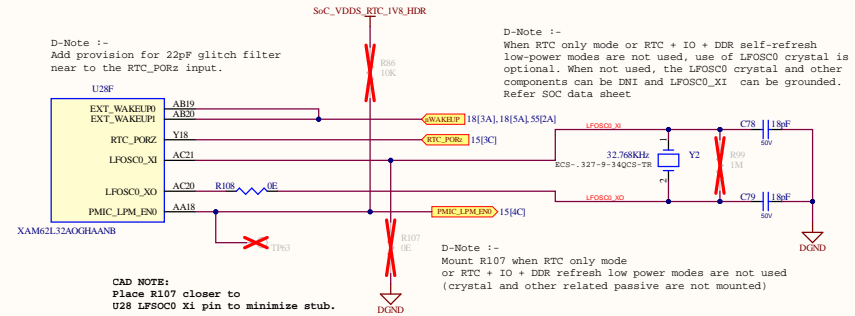


D-Note:-
The processor performance has been validated only with a 25 MHz Crystal/clock source connected to WKUP_OSC0 (25 MHz is the only clock frequency supported). The data sheet shows WKUP_OSC0 not starting until after the core voltage because there are some cases where the oscillator may not start until VDD_CORE is valid. In most cases the oscillator will start as early as VDDSYS_OSC0, but this may not always be the case. This diagram in the data sheet is showing the maximum start-up time, which must include the case where the delay is based on VDD_CORE being valid.

D-Note:-
The recommendation is to connect the 25 MHz crystal directly to the SOC XI and XO pins (no series or parallel resistors are recommended). The internal oscillator implements AGC (Automatic Gain Control) for amplitude control. The recommendation is to match the the SOC crystal and the EPHY crystal specifications

D-Note :-
No WKUP_OSC0 registers are required to be changed. These registers should remain in their default state. Select the appropriate crystal circuit components that are compliant to the values defined in the WKUP_OSC0 Crystal Circuit Requirements table. Read the Load Capacitance and Shunt Capacitance sections to select the appropriate crystal circuit components.

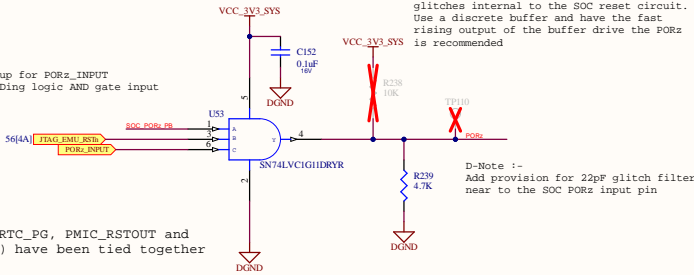
SOC RTC DOMAIN



SOC RESET

POWER ON RESET

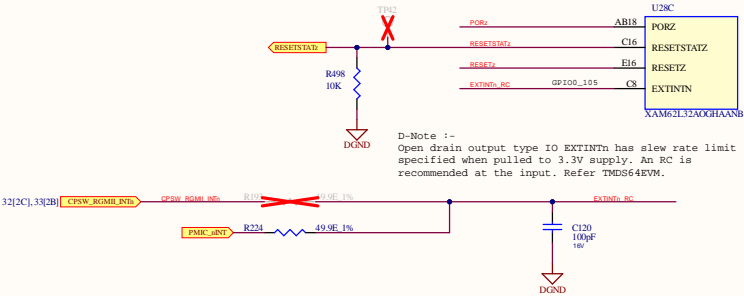
D-Note :-
Place the pullup for PORz_INPUT
near to the ANDing logic AND gate input



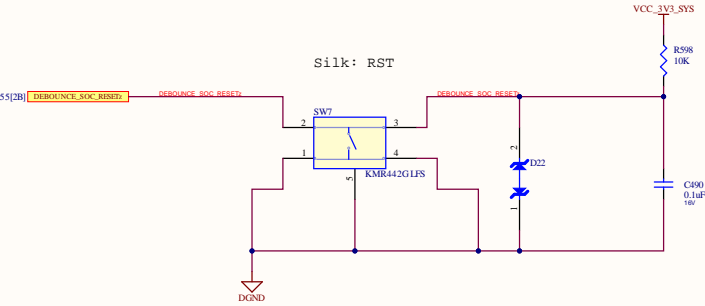
Note on Open-drain outputs:
XDS_PORzn, VCC_3V3_MAIN_PG, RTC_PG, PMIC_RSTOUT and
PMIC1_GPIO (5 output signals) have been tied together
as PORz_INPUT

D-Note :-
PORz input is 3.3V tolerant.
PORz ANDing logic AND gate supply is connected to
VCC_3V3_SYS. This is within the PORz fail-safe input range.

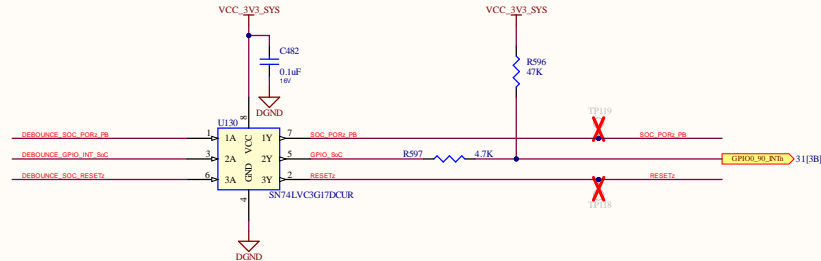
SOC - RESET



SOC WARM RESETz PUSH BUTTON

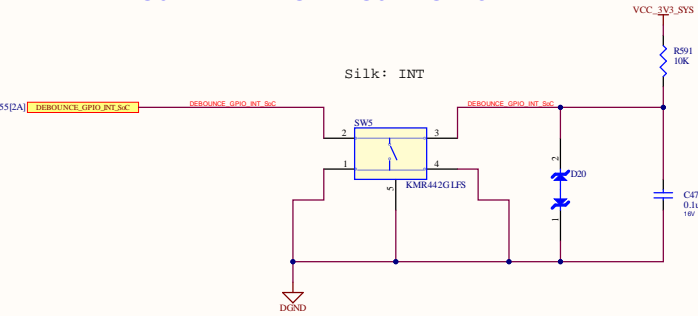


RESET & INT DEBOUNCE CIRCUIT

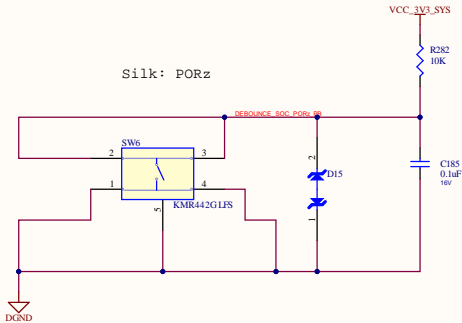


Processor LVCMOS I/Os (inputs) have slew rate requirement specified.
A Schmitt trigger based debouncing logic is recommended for the slow ramp
pushbutton output (+ RC) connected to the processor warm reset inputs.
Debouncing logic is recommended when push button + RC or RC is used at the
LVCMOS inputs.

USER INTERRUPT PUSH BUTTON



SOC PORz RESET PUSH BUTTON



BOOT MODE SWITCHES

D-NOTE:

The device supports the following BOOTMODE pin mapping options:

1. Reduced Pincount - Using only 4 of the bootstrap pins BOOTMODE[15:12]
2. Full Pincount - Using all 16 of the bootstrap pins BOOTMODE[15:0]
3. Configuring the reduced pincount bootmode resistors to boot from eFuse

FULL PINCOUNT SWITCHES

D-Note :-

To reduce the number of resistors used for bootmode configuration (pullup/pulldown) when using reduced pin count bootmode, the input buffers for BOOTMODE[11:0] inputs (pins) are disabled during POR (cold reset) unless BOOTMODE[15:14] are configured as '00' (Full Pincount bootmode).

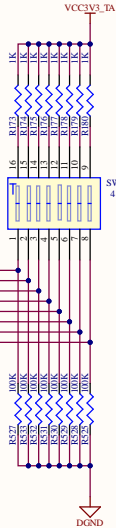
D-Note:

VCC3V3_TA supply is used for bootmode configuration to support test automation. The recommendation is to connect to SoC_DVDD3V3 on the custom board design when test automation or bootmode buffers are not used.

SWITCH ON = LOGIC 1
SWITCH OFF = LOGIC 0

Silk: BMODE 0-7

44[1B],44[0] <SYS_BOOTMODE>
44[1B],44[1] <SYS_BOOTMODE>
44[1B],44[2] <SYS_BOOTMODE>
44[1B],44[3] <SYS_BOOTMODE>
44[1B],44[4] <SYS_BOOTMODE>
44[1B],44[5] <SYS_BOOTMODE>
44[1B],44[6] <SYS_BOOTMODE>
44[1B],44[7] <SYS_BOOTMODE>

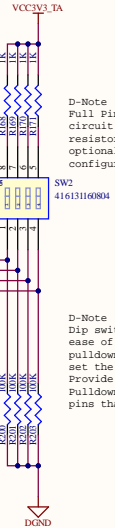


Silk: BMODE 8-11

44[3B],44[8] <SYS_BOOTMODE>
44[3B],44[9] <SYS_BOOTMODE>
44[3B],44[10] <SYS_BOOTMODE>
44[3B],44[11] <SYS_BOOTMODE>

D-Note :-
When dip switches are used on custom board, an external ESD protection may be required if the DIP switches are expected to be configured in an uncontrolled ESD environment

D-Note :-
When DIP switches are used, reduce the resistor values used for the divider to 47K and 470R maintaining the ratio (for improved noise performance)

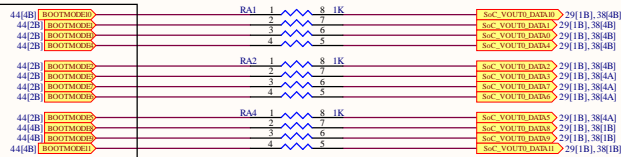


D-Note :-
Full Pincount bootmode configuration circuit including pullup, pulldown resistors and DIP switches, buffers are optional when reduced pincount bootmode configuration is used

D-Note :-
Dip switch is optional and used for ease of configuration. A pullup or pulldown resistor can be used to set the BOOTMODE configuration. Provide provision for Pullup and Pulldown resistors for the bootmode pins that have configuration capability

BOOTMODE PINS

Signals from Bootmode buffer



D-Note :-
Connect SYS_BOOTMODE signals when bootmode buffers are not used

D-NOTE:
1. 1K Resistor at the output of the buffer is recommended
2. Replace 1K Resistor at the output of the buffer with resistor of value 0R when bootmode buffers are not used

BOOT MODES SUPPORTED

1. eMMC
2. OSPI
3. MMC1 - uSD Card
4. UART
5. USB0 DFU
6. USB0 MS

FAQs FOR BOOTMODE CONFIGURATION (WITH BUFFER OR WITHOUT BUFFER)

<https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1391522/faq-am625-am623-am644x-am243x-am62a-am62p-am62d-q1-am62l---bootmode-implementation-without-buffers>

<https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1414148/faq-am625-am623-am644x-am243x-am62a-am62p-am62d-q1-am62l---bootmode-implementation-with-buffers>

REDUCED PINCOUNT SWITCH

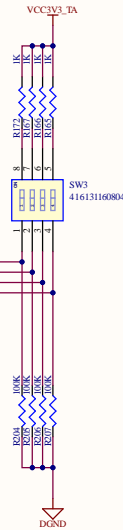
D-Note :-

Boot from eFuse can be configured using the reduced pin count bootmode configuration.

SWITCH ON = LOGIC 1
SWITCH OFF = LOGIC 0

Silk: BMODE 12-15

44[3D],44[5B] <SYS_BOOTMODE>
44[3D],44[6B] <SYS_BOOTMODE>
44[3D],44[7B] <SYS_BOOTMODE>
44[3D],44[8B] <SYS_BOOTMODE>



BOOTMODE PINS

Signals from Bootmode buffer

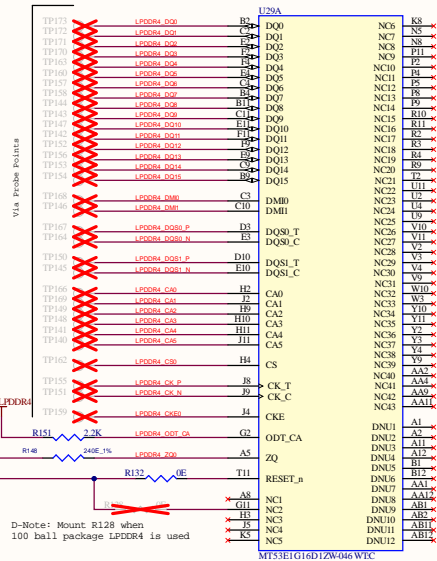


D-Note :-
Connect SYS_BOOTMODE signals when bootmode buffers are not used

D-NOTE:
1. 1K Resistor at the output of the buffer is recommended
2. Replace 1K Resistor at the output of the buffer with resistor

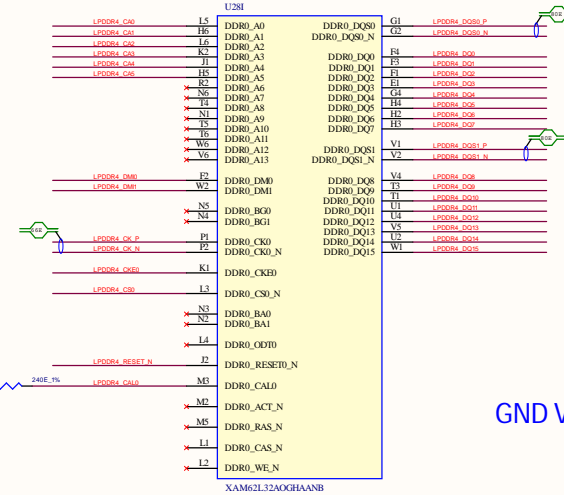
LPDDR4 DEVICE

Silk: LPDDR4

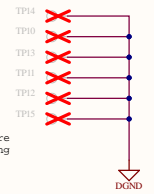


D-Note :-
Use 10K pulldown for the LPDDR4 attached device reset signal (pin) LPDDR4_RESET_N
Refer processor family specific DDR design guide

SOC LPDDR4 INTERFACE

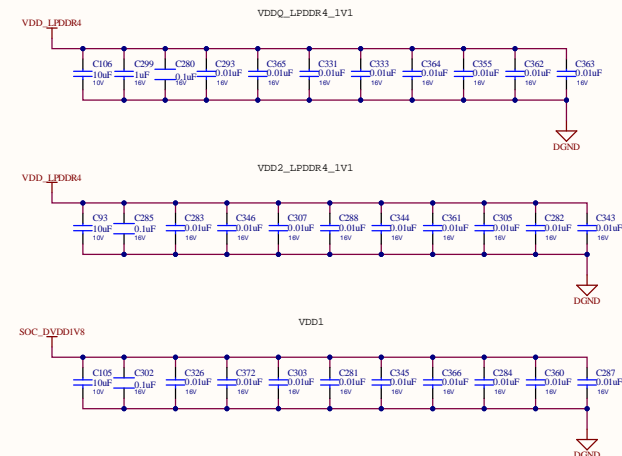
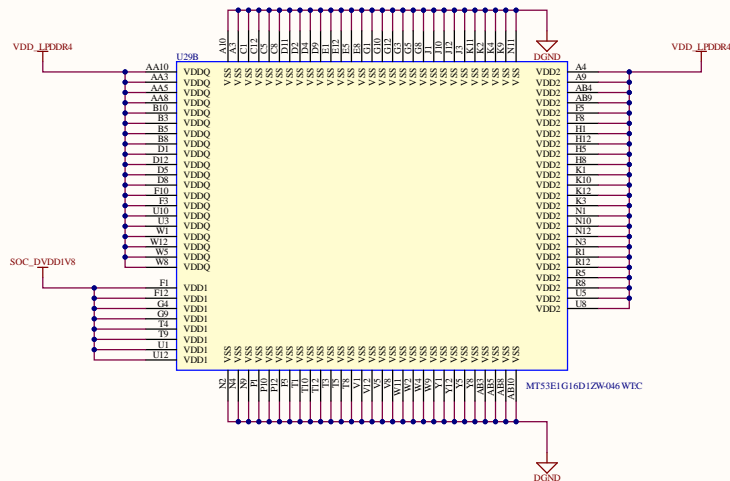


GND VIA PROBE POINTS



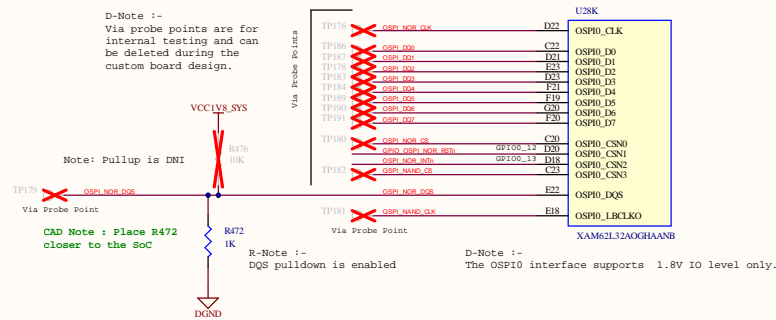
D-Note :-
Via probe points are for internal testing and can be deleted during the custom board design.

LPDDR4 POWER DECAPS

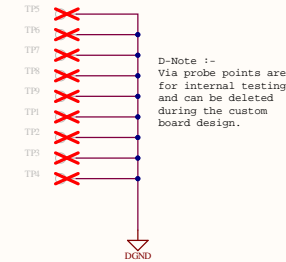


Title		
Size A4	Number PROC181E-1	Revision
Date: 7-10-2025	Sheet of	
File: D:\Arvind\124SchDoc	Drawn By:	

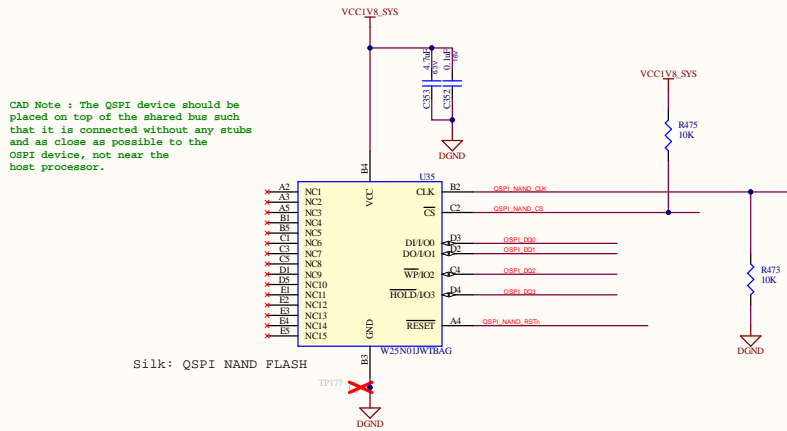
SOC OSPI INTERFACE



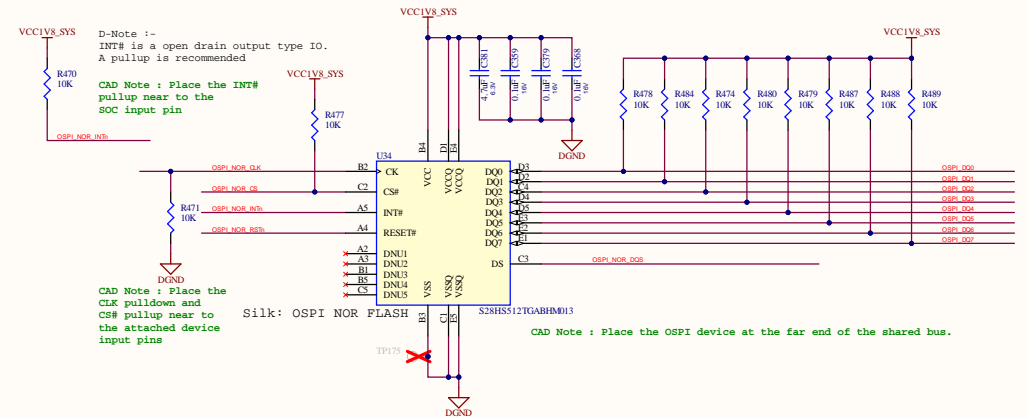
GND VIA PROBE POINTS



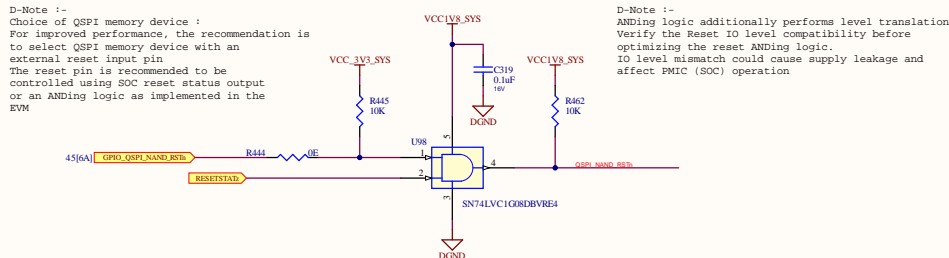
OSPI NAND FLASH



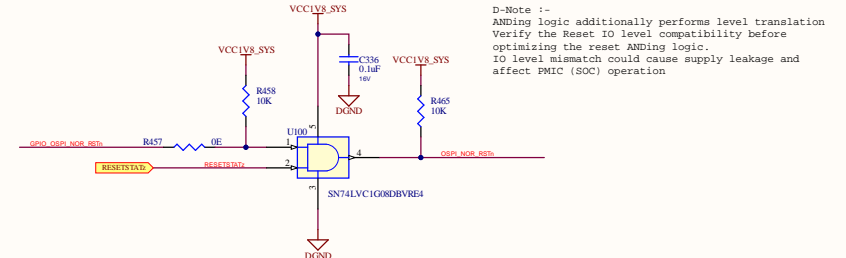
OSPI NOR FLASH



OSPI NAND FLASH RESET



OSPI NOR FLASH RESET



FAQ REFERENCE

<https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1484438/faq-am62l-custom-board-hardware-design-ospio-interface-implementation-on-tmds62levm-guidelines>

Title		
Size	Number	Revision
A4	PROC181E1-1	
Date:	7-10-2025	Sheet of
File:	D:\Arvind_05\SchDoc	Drawn By:

eMMC INTERFACE

D-Note :
The processor I/Os associated with the MMC0 port will be turned off until software initializes them. This means any signals without internal pulls will be floating until software boots and initializes the I/Os.
The JEDEC eMMC electrical standard v5.1 (JESD84-B51) requires the eMMC device to have internal pulls on the DAT[7:1] pins, but the other pins do not have internal pulls.
We recommend external pull-ups on the CMD and DAT0 signals and an external pull-down on the CLK signal. The eMMC standard also says 10k pull-ups are the min value, so we do not recommend using a 10k resistor because it may be less than 10k. We typically recommend using 47k resistors to minimize loading on the signals since the pulls are only used to hold the signals in a valid logic state when not driven.

D-Note:-
The processor family implements a soft PHY for eMMC interface. The pulls required for D0, Clock and other eMMC interface control signals are recommended to be implemented externally

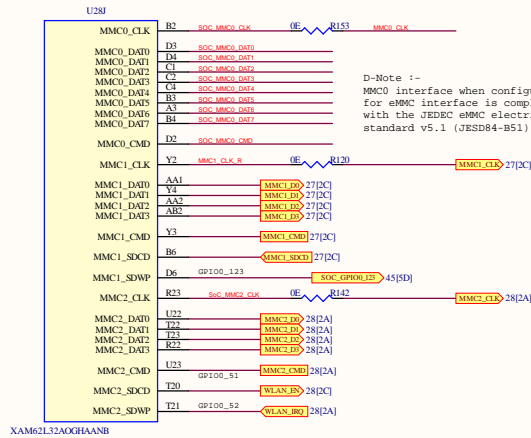
D-Note:-
The JEDEC eMMC electrical standard v5.1 (JESD84-B51) requires all eMMC devices to have an internal pull-up that is turned on by default for each DAT[7:1] pin. The eMMC device will turn off the internal pulls on DAT[7:1] when it is configured to operate in 8-bit mode or turn off the internal pulls on DAT[3:1] when it is configured to operate in 4-bit mode. The software driver should turn on the respective AM62x internal pull-ups at the same time it configures the eMMC device to operate in 8-bit mode or 4-bit mode. This ensures the signals are not floating when not driven.
External pull-ups are not necessary on the DAT[7:1] signals as long as the software driver is turning on the respective AM62x pull-ups at the appropriate time.

eMMC FLASH

SOC - MMC Interface

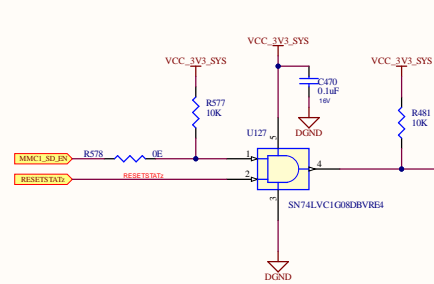
D-Note :
Series resistor (OE) provision on MMC0_CLK is recommended to control reflections (for addressing signal integrity related concerns)

D-Note :-
MMC0 interface when configured for eMMC interface is compliant with the JEDEC eMMC electrical standard v5.1 (JESD84-B51)



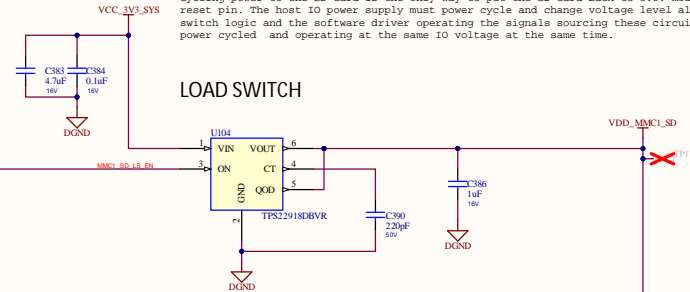
SD CARD INTERFACE

SD CARD RESET



D-Note :-
The SD card supply control power switch, the power switch supply output (EN) reset logic, and the host IO power supply circuit are required to support UHS-I SD Cards which begins communications using 3.3V signal levels and later switches to 1.8V signal levels when configuring to one of the faster data transfer speeds.
Cycling power to the SD Card is the only way to put the SD card back to 3.3V mode since SD Cards do not have a reset pin. The host IO power supply must power cycle and change voltage level along with the SD Card. The Power switch logic and the software driver operating the signals sourcing these circuits ensure both devices are power cycled and operating at the same IO voltage at the same time.

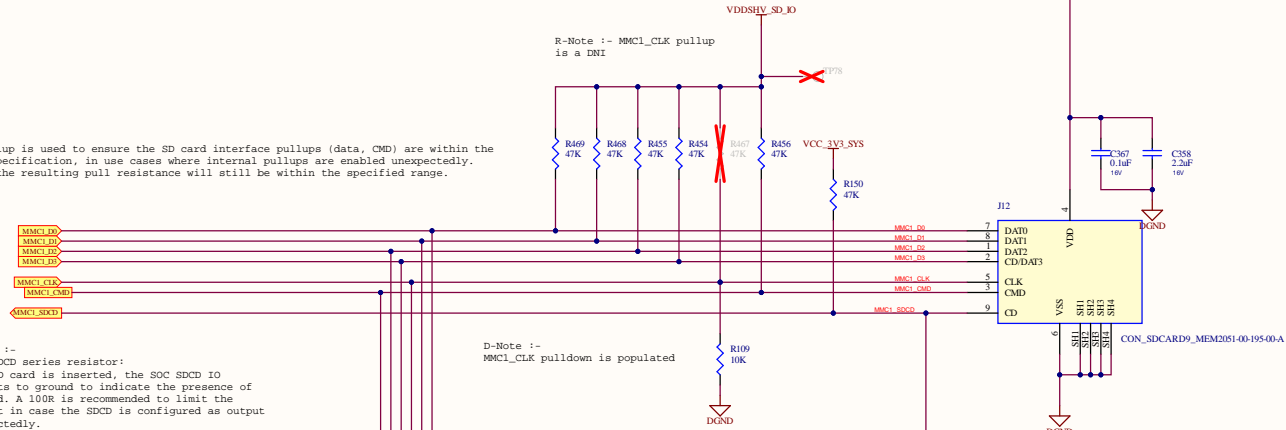
LOAD SWITCH



D-Note :-
To support UHS-I SD Card interface, the pullups are recommended to be connected to the 3.3V/1.8V switched LDO output (can be the integrated LDO output)

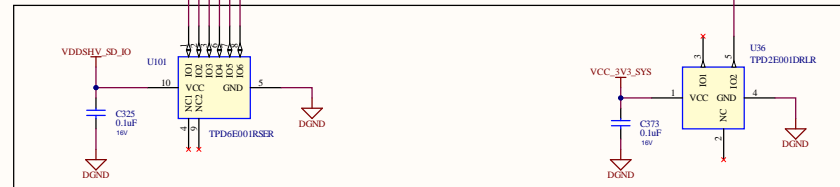
R-Note :- MMCI_CLK pullup is a DNI

D-Note :-
A 47K pullup is used to ensure the SD card interface pullups (data, CMD) are within the SD card specification, in use cases where internal pullups are enabled unexpectedly. This way the resulting pull resistance will still be within the specified range.



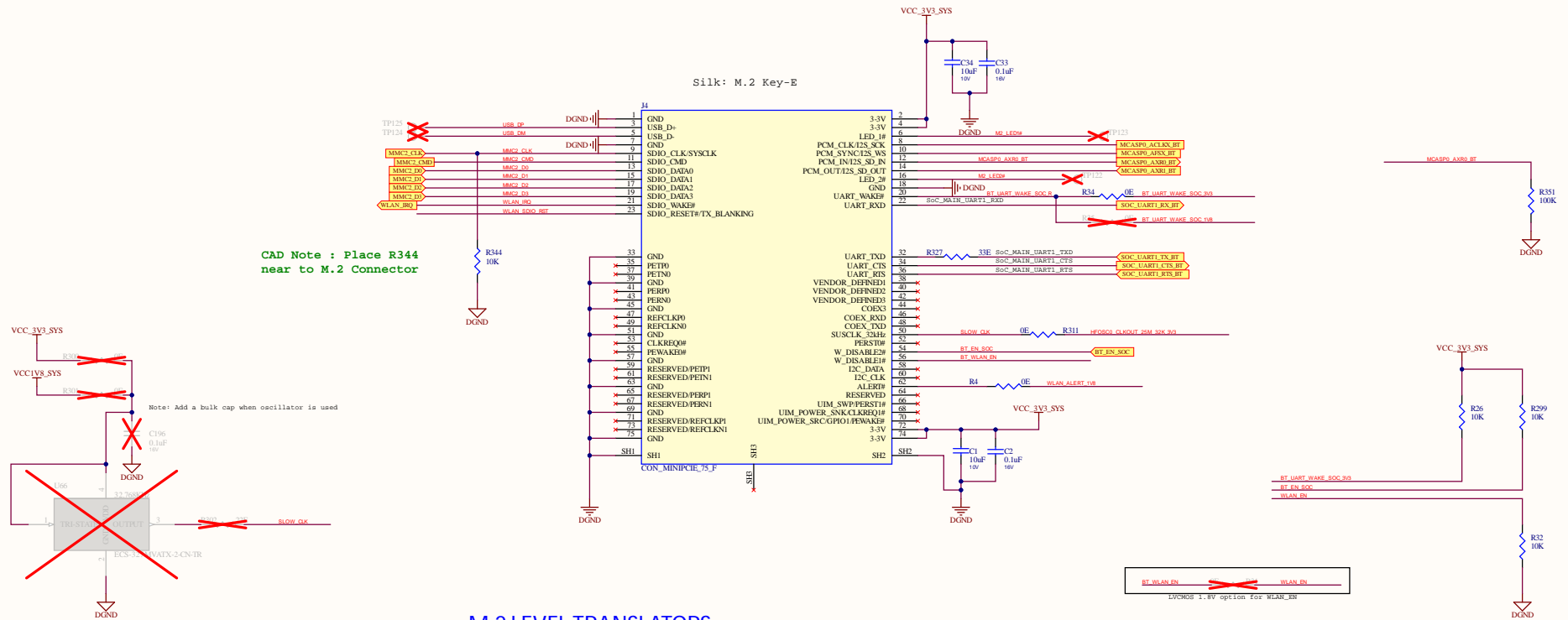
D-Note :-
MMC1_SDCD series resistor:
When SD card is inserted, the SOC SDCD IO connects to ground to indicate the presence of SD card. A 100R is recommended to limit the current in case the SDCD is configured as output unexpectedly.

D-Note :-
MMC1_CLK pulldown is populated

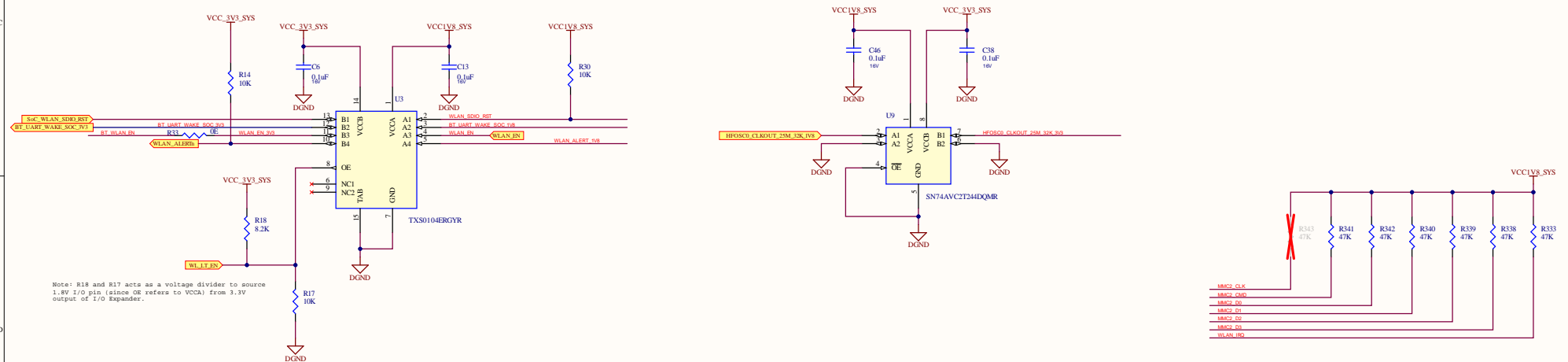


CAD Note : Place external ESD protection near to SD Card Connector

M.2 INTERFACE - SDIO



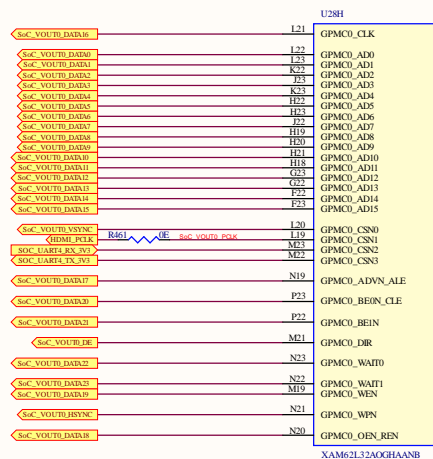
M.2 LEVEL TRANSLATORS



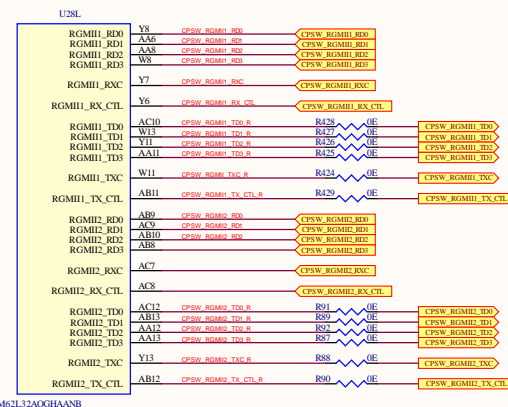
Title			
Size	Number	Revision	
A4	PROC181E1-1		
Date:	7-10-2025	Sheet of	
File:	D:\Arvind_28SchDoc	Drawn By:	

D-Note:- Shorting of multiple bootmode inputs together is not recommended or allowed, since the bootmode inputs have alternate functions that could be configured after boot (can be set as outputs) Shorting the bootmode pins directly to VCC or ground directly is not recommended. Connect each of the bootmode pins through separate resistor. Choose the bootmode resistor value based on the use case (10K or similar)

SOC - GPMC

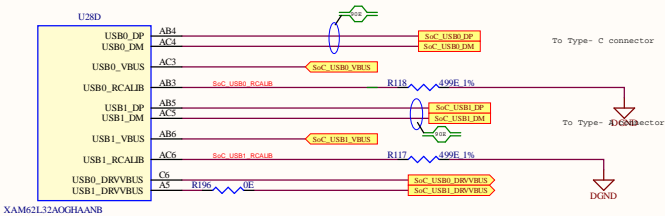


SOC - ETHERNET INTERFACE

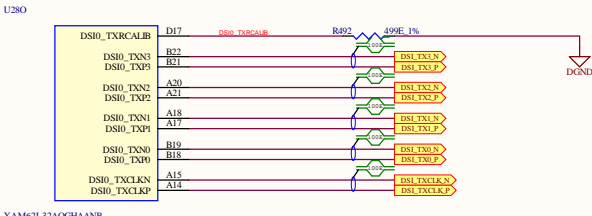


XAM62L32AOGHAANB

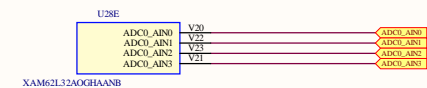
SOC - USB



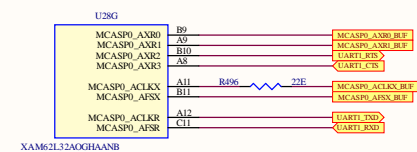
SOC - DSI



SOC - ADC

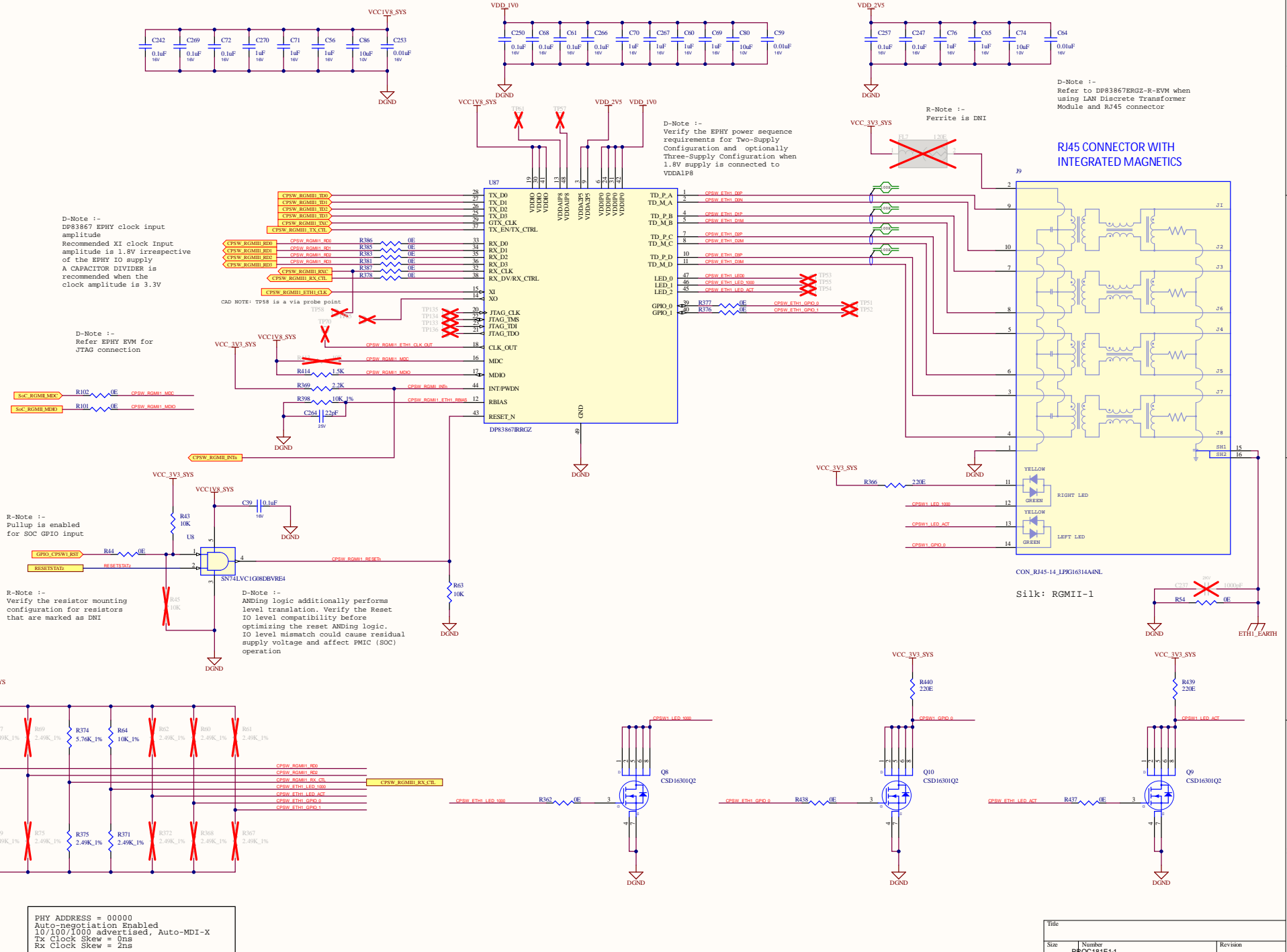


SOC - MCASP and UART



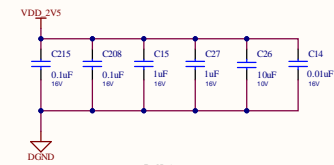
CPSW3G RGMII_1 ETHERNET PHY

D-Note :-
The caps and values used are as per the EPHY datasheet recommendations.

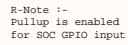


Title		
Size A4	Number PROC181E1-1	Revision
Date: 7-10-2025	File: D:\Arvind\332 SchlDoc	Sheet of Drawn By:

D-Note :-
The caps and values used are as per the EPHY data sheet recommendations.

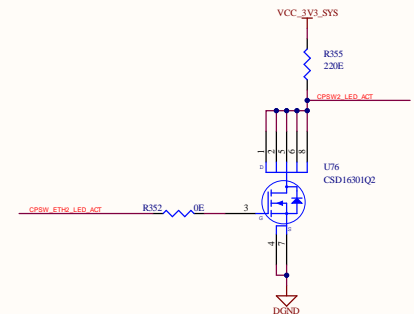
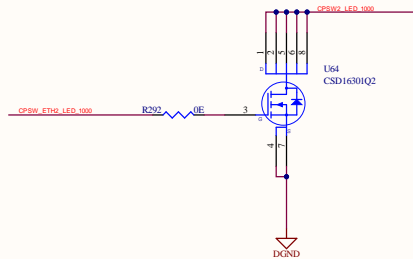


R-Note :-
Ferrite is DNI

RJ45 CONNECTOR WITH
INTEGRATED MAGNETICS

R-Note :-
Verify the resistor mounting configuration for resistors that are marked as DNI

D-Note :-
ANDING logic additionally performs level translation. Verify the Reset IO level compatibility before optimizing the reset ANDING logic.
IO level mismatch could cause supply leakage and affect PMIC (SOC) operation

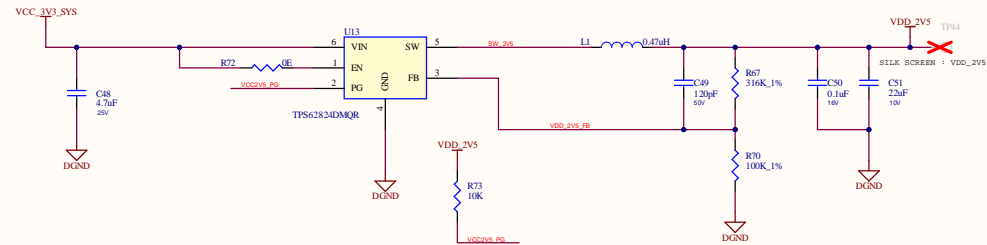


Silk: RGMII-2

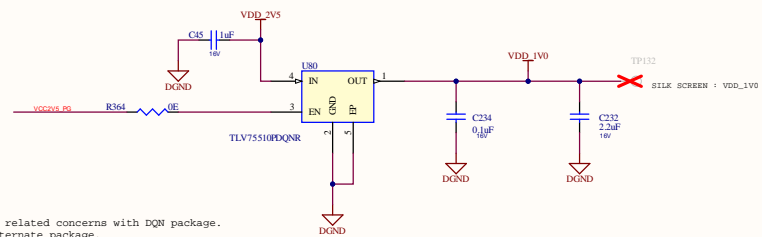
Title		
Size A4	Number PROC181E-1	Revision
Date: 7-10-2025	Sheet of	
File: D:\Arvind\133\SchDoc	Drawn By:	

POWER SUPPLY (CORE) FOR ETHERNET PHY

2.5V (ETHERNET PHY), 1.0AMPS SUPPLY

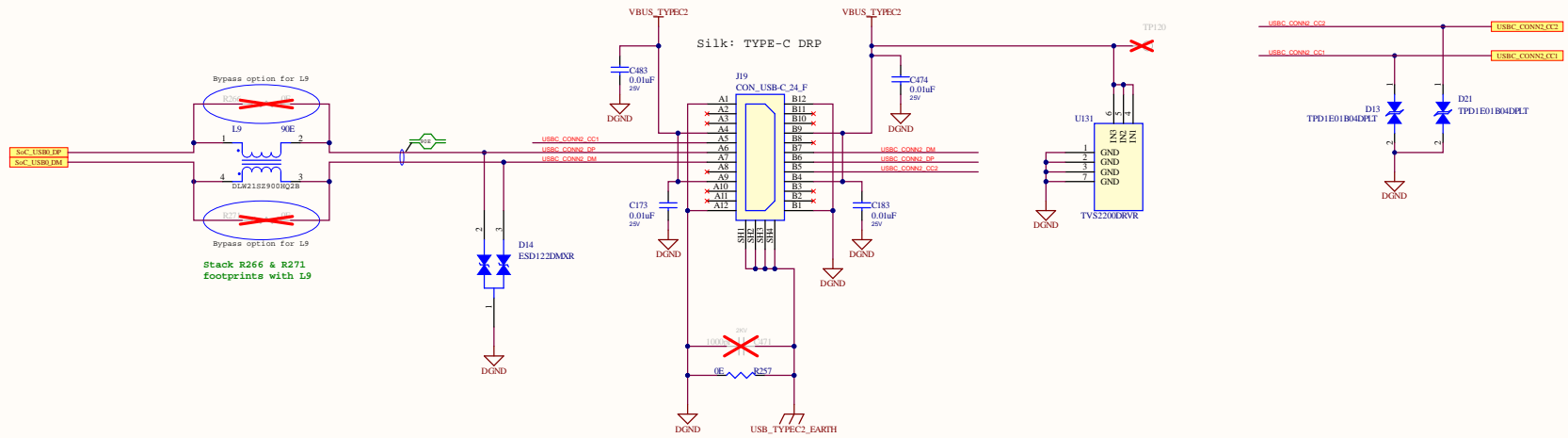


1.0V (ETHERNET PHY), 0.5AMPS SUPPLY

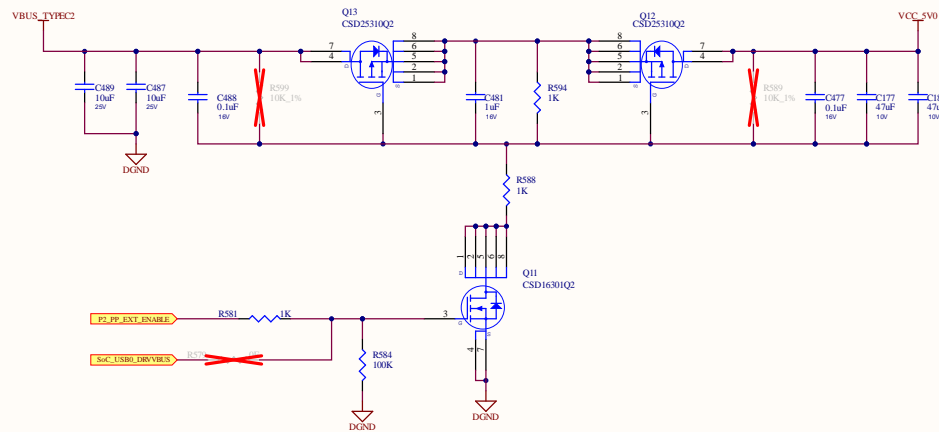


D-Note :-
Note the assembly related concerns with DQNR package.
Consider using alternate package.

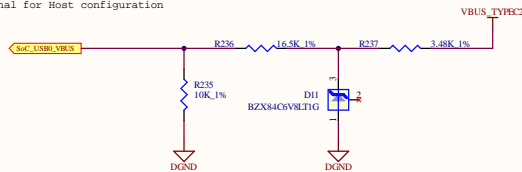
USB0 TYPE-C DRP



EXTERNAL POWER PATH FOR SOURCING, 5V/0.5A



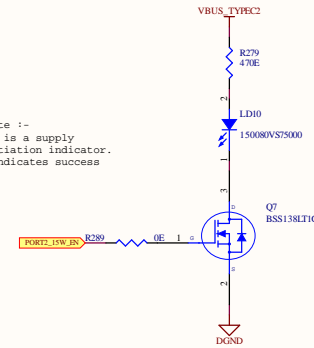
D-Note :-
VBUS connection is optional for Host configuration



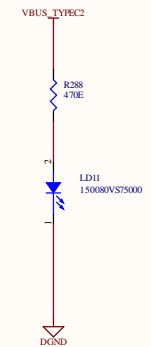
D-Note :-
Refer USB VBUS Design Guidelines section of SOC data sheet

PORT2_15W_EN STATUS INDICATION LED

R-Note :-
This is a supply
negotiation indicator.
ON indicates success

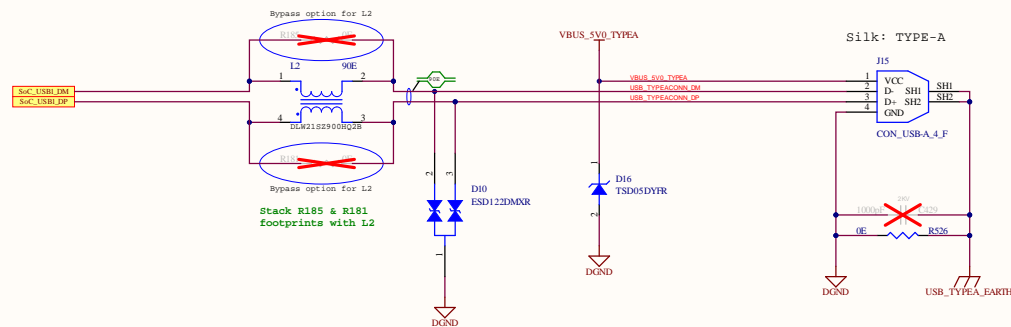
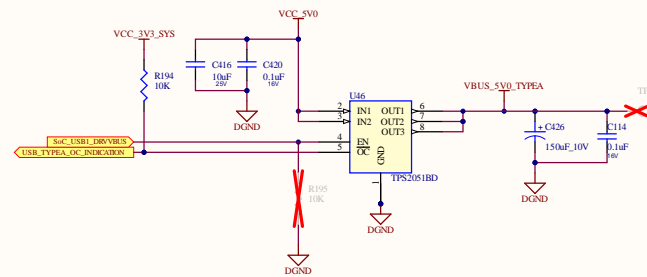


POWER INDICATION LED: VBUS_TYPEC2

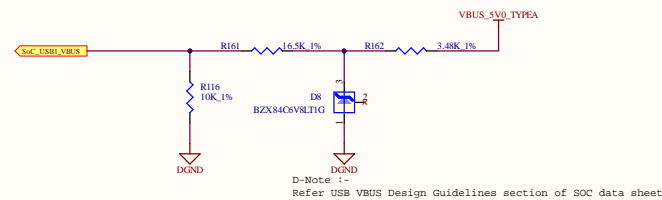


Title			Revision
Size	Number	Revision	
A4	PROC181E1-1		
Date:	7-10-2025	Sheet of	
File:	D:\Arvind\135SchDoc	Drawn By:	

USB1 TYPE-A

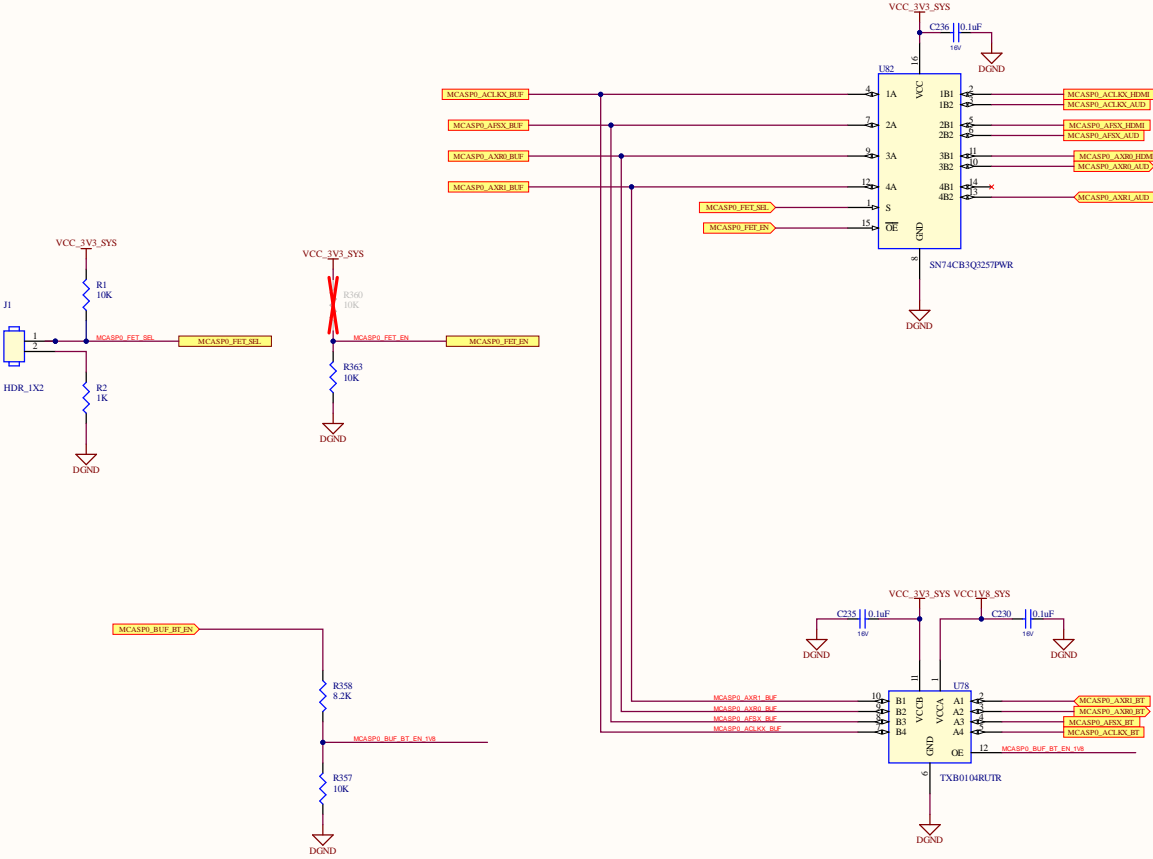


D-Note :-
VBUS connection is optional for Host configuration

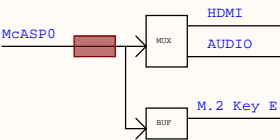


Title		
Size A4	Number PROC181E1-1	Revision
Date: 7-10-2025	Sheet of	
File: D:\Arvind\...36.Sch.Doc	Drawn By:	

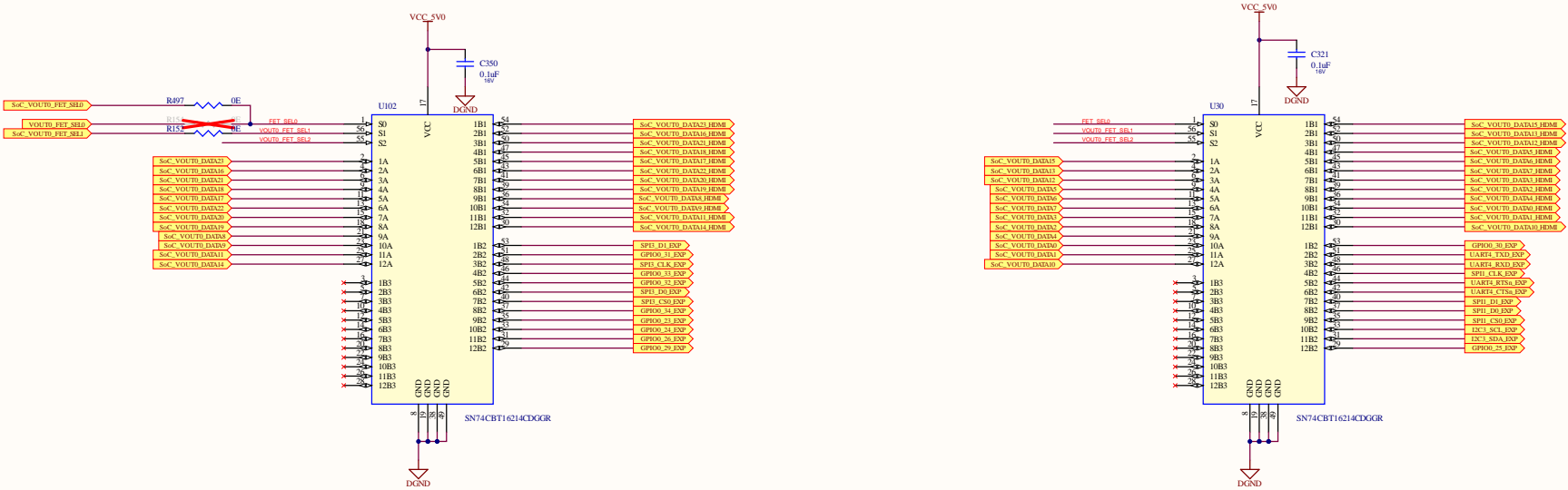
SOC MAIN McASP0 FET BUS SWITCH & VOLTAGE LEVEL TRANSLATOR



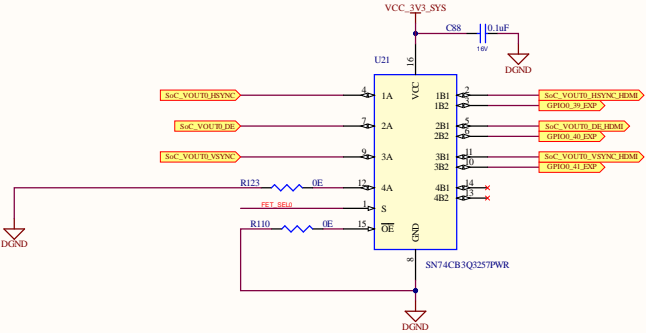
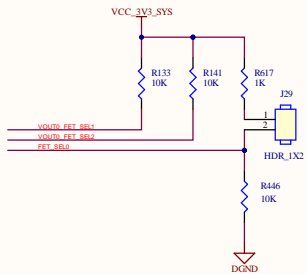
OEn	SEL	INPUT/OUTPUT	
		nA	
L	H(DEFAULT)	nA=nB2	MCASP0 - CODEC
L	L	nA=nB1	MCASP0 - HDMI



SoC_VOUTO FET SWITCHES



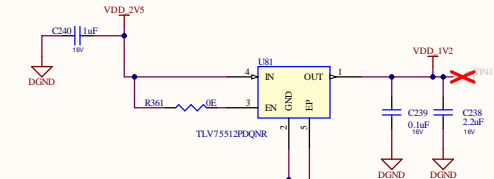
S2	S1	S0	INPUT/OUTPUT nA	
H	H	L	nA=nB1	SOC - HDMI (DEFAULT)
H	H	H	nA=nB2	SOC - GPIO EXP CONN



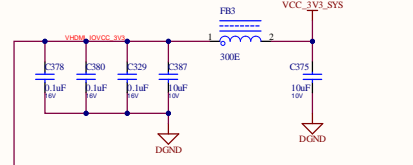
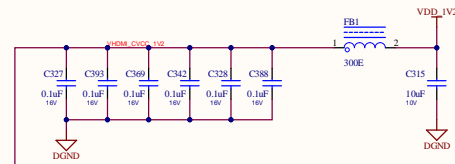
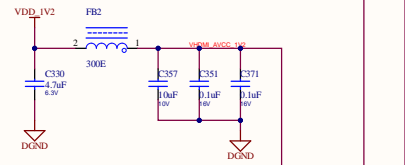
OEn	SEL	INPUT/OUTPUT nA	
L	L	nA=nB1	SOC - HDMI (DEFAULT)
L	H	nA=nB2	SOC - GPIO EXP CONN

HDMI INTERFACE

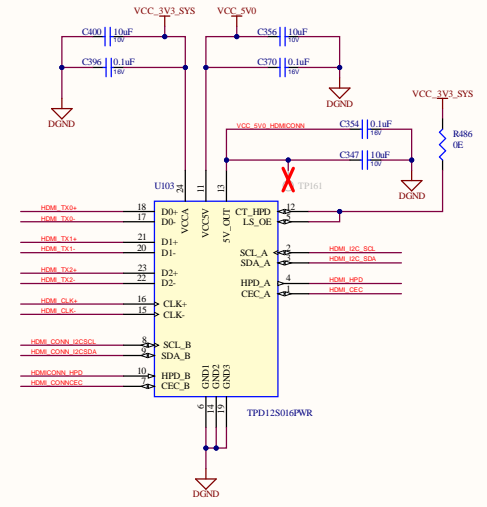
1.2V (HDMI), 0.5AMPS SUPPLY



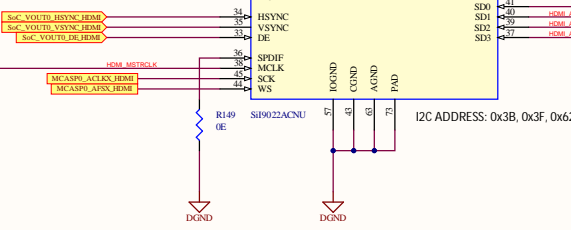
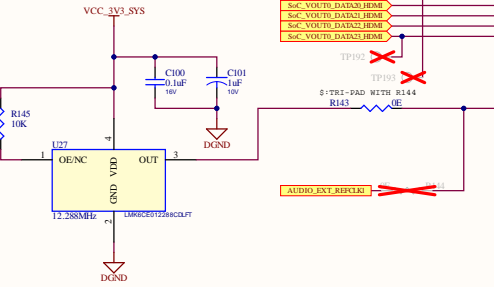
D-Note :-
Note the assembly related concerns with DQN package.
Consider using alternate package.



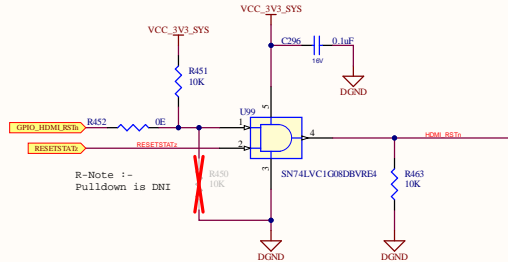
HDMI ESD DEVICE



NOTE:
TPD12S016PWR has integrated pullup or pulldown resistors on the I2C and HPD lines hence no external pullup or pulldown required.

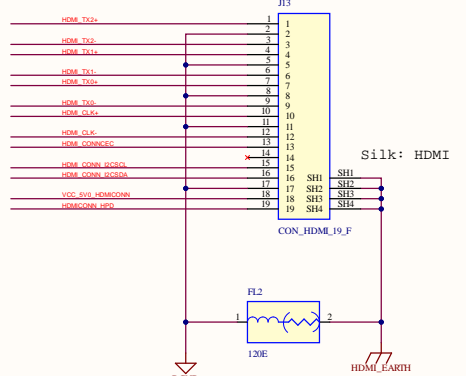


HDMI RESET



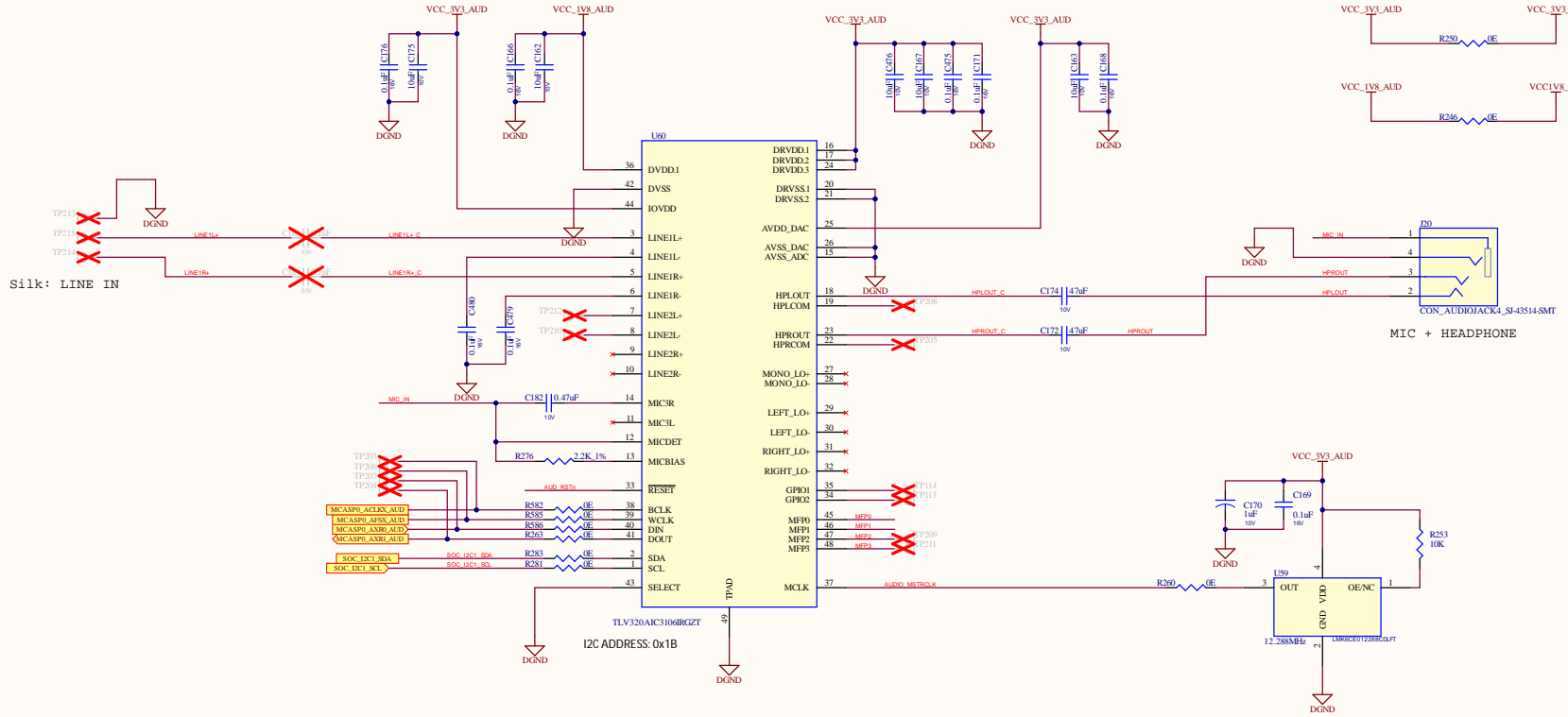
R-Note :-
Pulldown is DNI

HDMI CONNECTOR

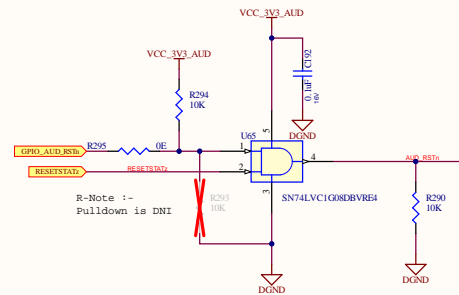


Title	
Size	Number
A4	PROC181E1-1
Date	7-10-2025
File	D:\Arvind_19\SchDoc
Revision	
Sheet of	
Drawn By:	

AUDIO CODEC

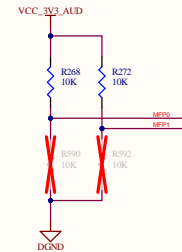


AUDIO CODEC RESET

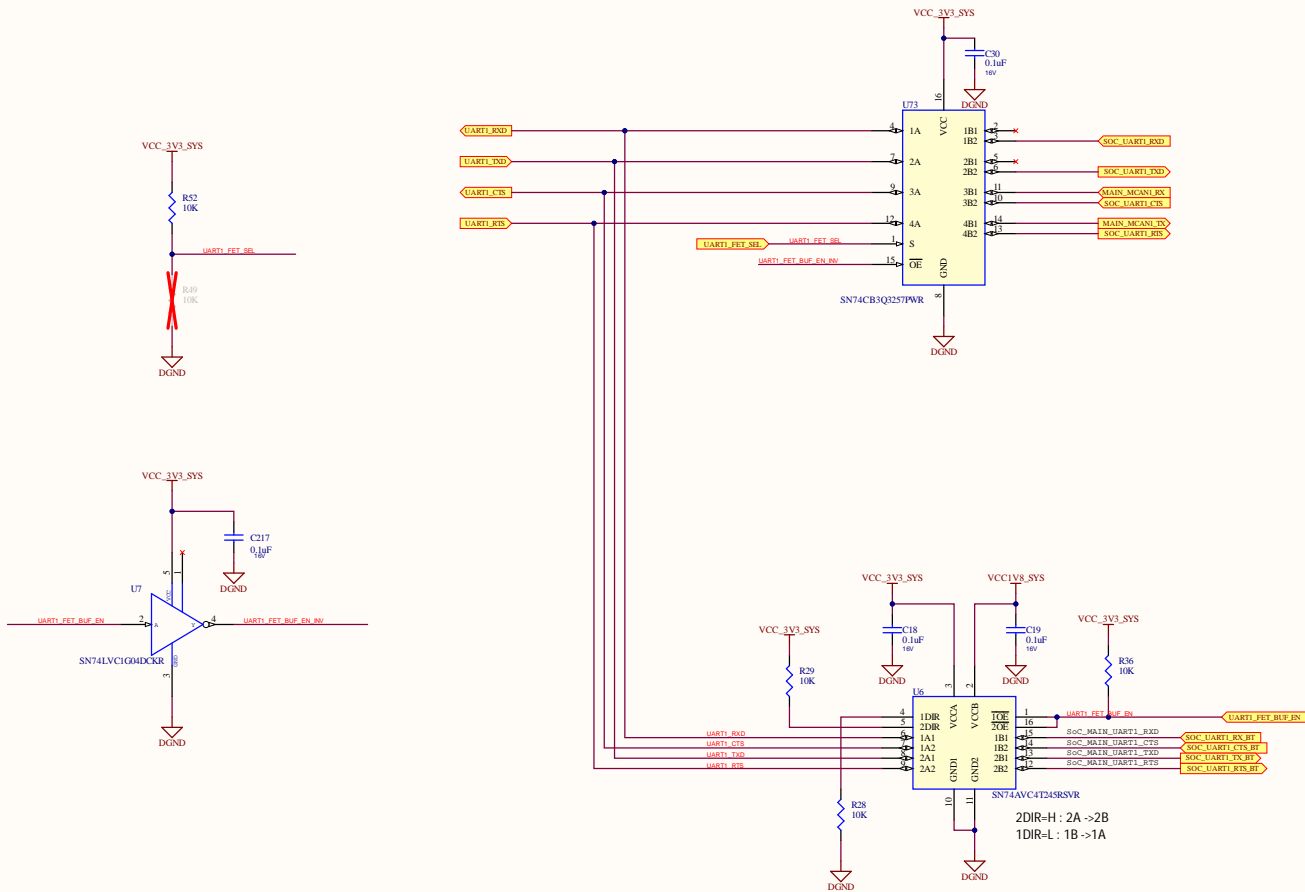


CODEC I2C ADDRESS SELECTION

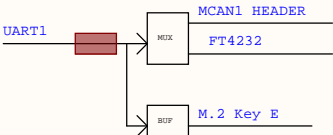
MPF0	MPF1	Device Address
0	0	0x18
0	1	0x19
1	0	0x1A
1	1	0x1B



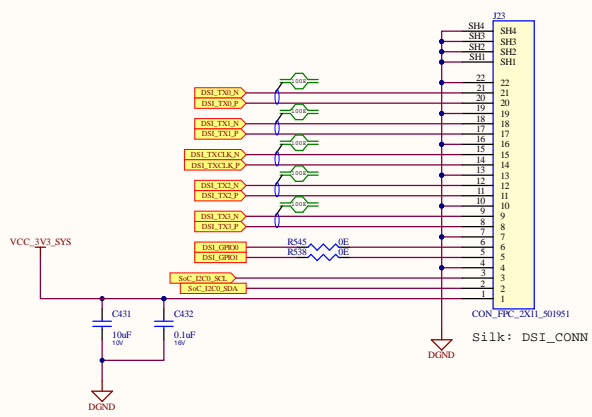
SOC MAIN UART1 - FET SWITCH & VOLTAGE LEVEL TRANSLATOR



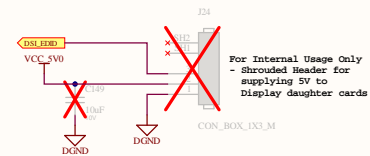
OEn	SEL	INPUT/OUTPUT	
		nA	nA
L	L	nA=nB1	SOC - MCAN1 HEADER
L	H(DEFAULT)	nA=nB2	SOC - FT4232



DSI INTERFACE

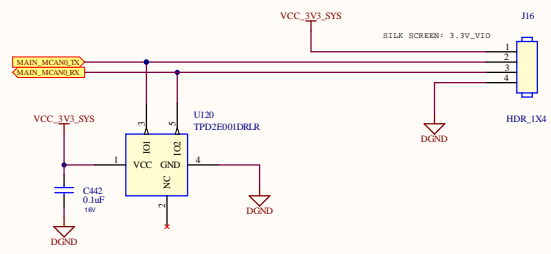


ADD ON CARD HEADER

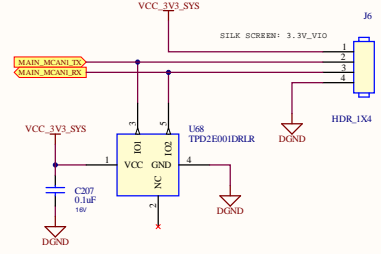


MCAN INTERFACE

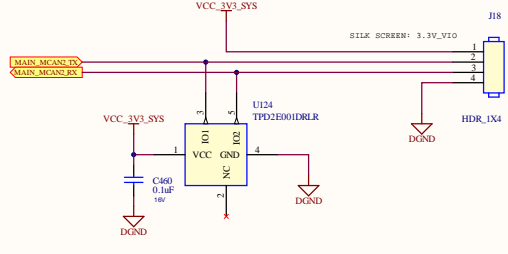
MCAN0 HEADER



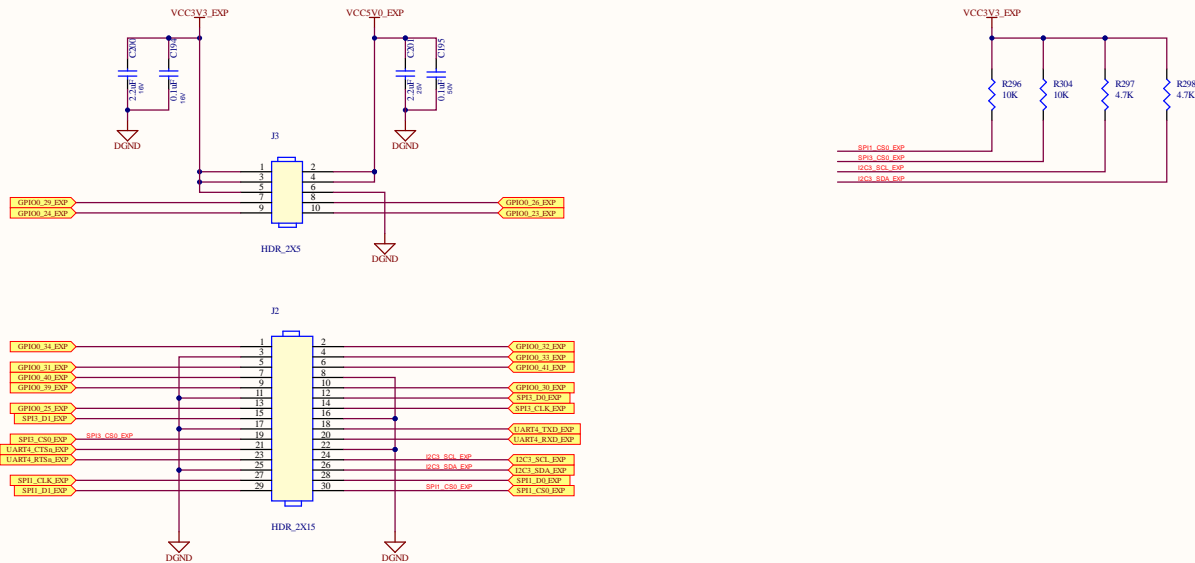
MCAN1 HEADER



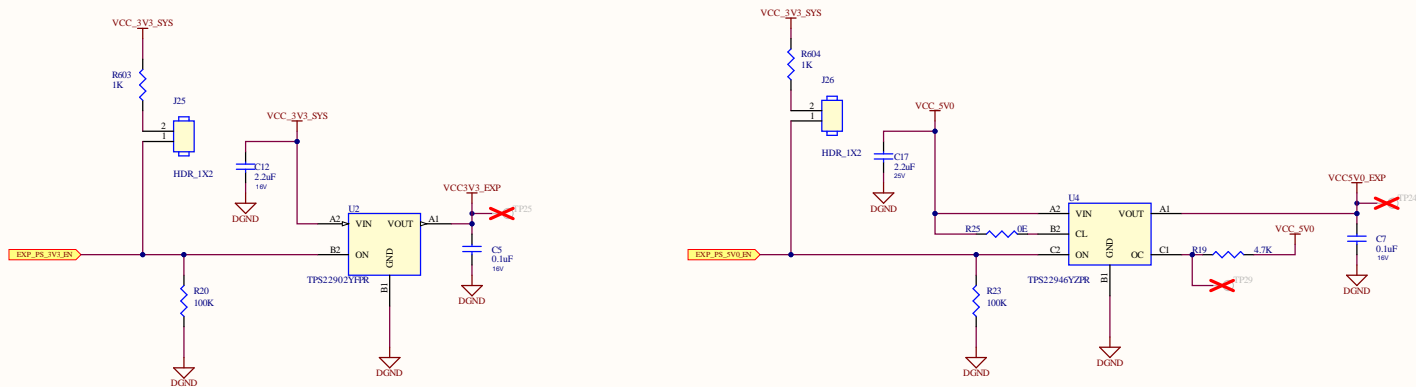
MCAN2 HEADER



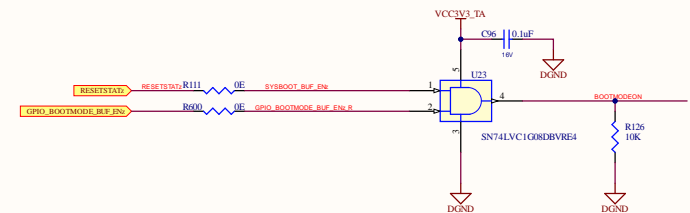
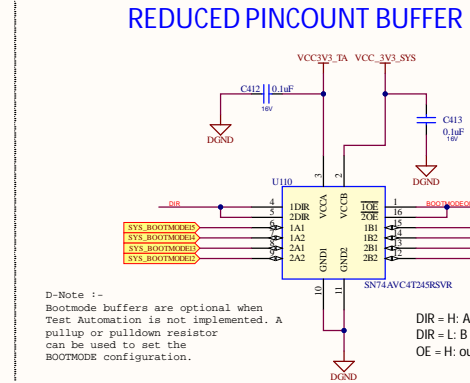
GPIO EXPANSION CONNECTOR



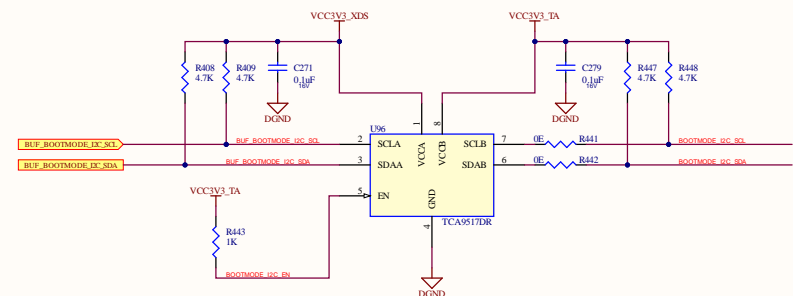
LOAD SWITCH FOR GPIO EXPANSION CONNECTOR



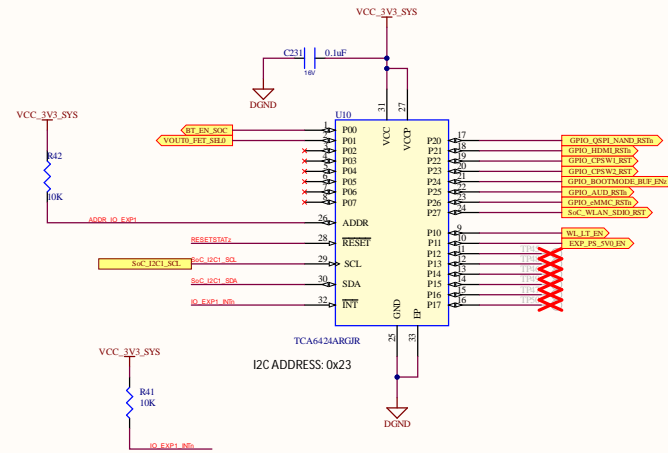
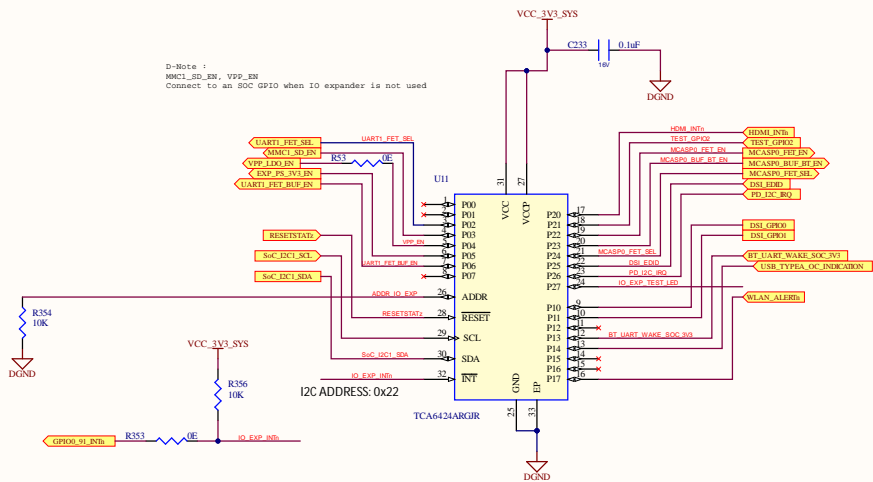
FULL PINCOUNT BUFFERS



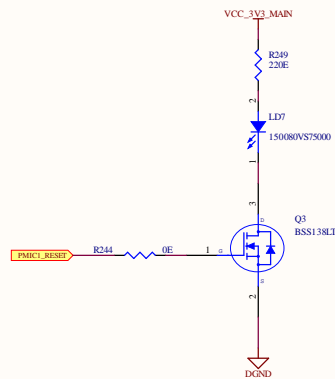
BOOTMODE I2C BUS BUFFER



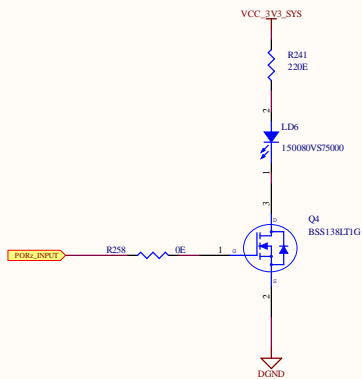
IO EXPANDERS



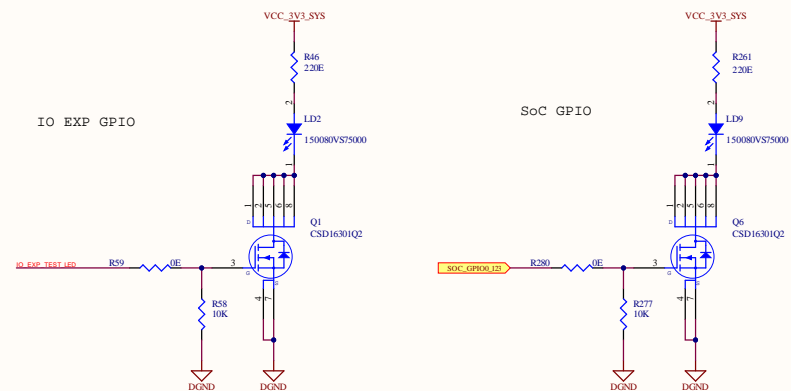
RTC ONLY MODE INDICATION LED



POWERGOOD INDICATION LED

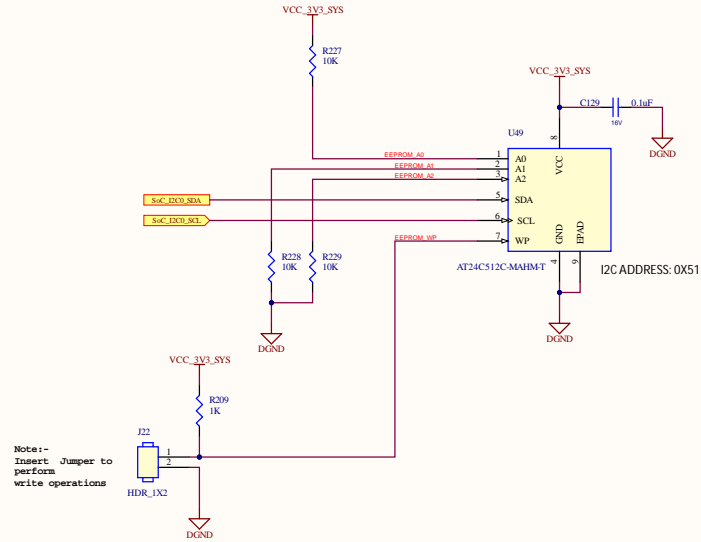


USER TEST LEDS



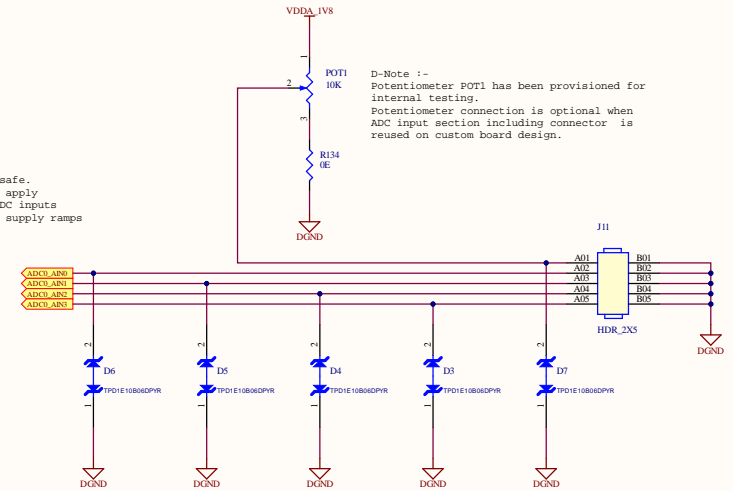
Title		
Size A4	Number PROC181E-1	Revision
Date: File:	7-10-2025 D:\Arvind\45 SchDoc	Sheet of Drawn By:

BOARD ID EEPROM

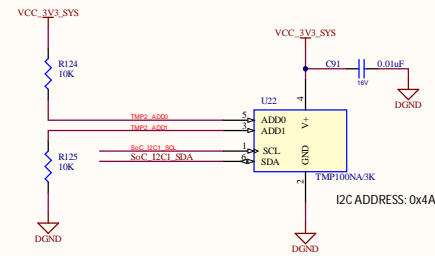
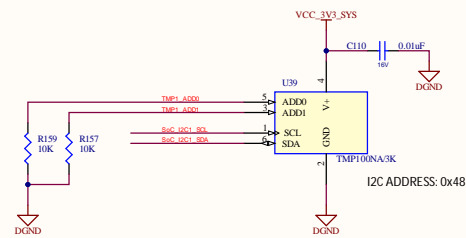


ADC INTERFACE

D-Note :-
ADC inputs are not fail-safe.
The recommendation is to apply
external inputs to the ADC inputs
only after the SOC ADC supply ramps



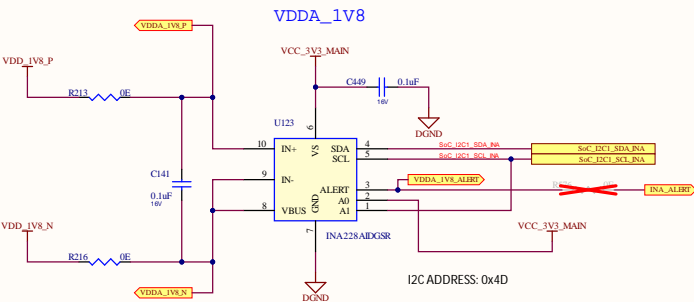
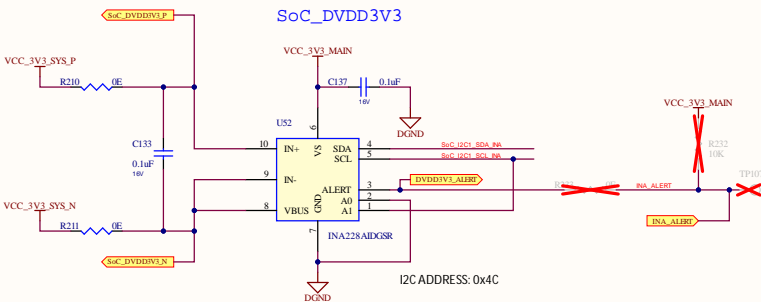
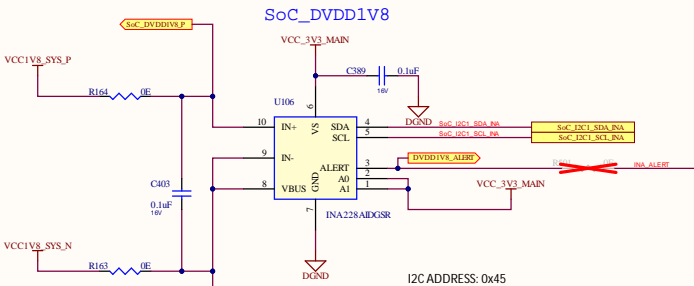
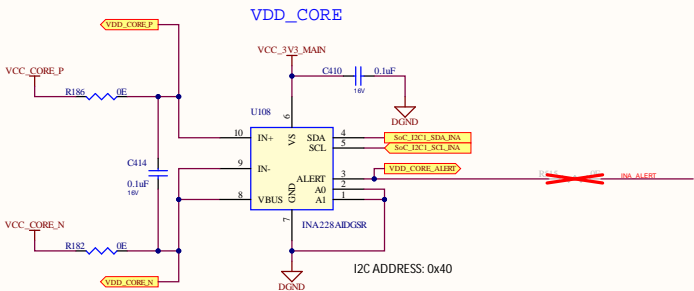
TEMPERATURE SENSORS



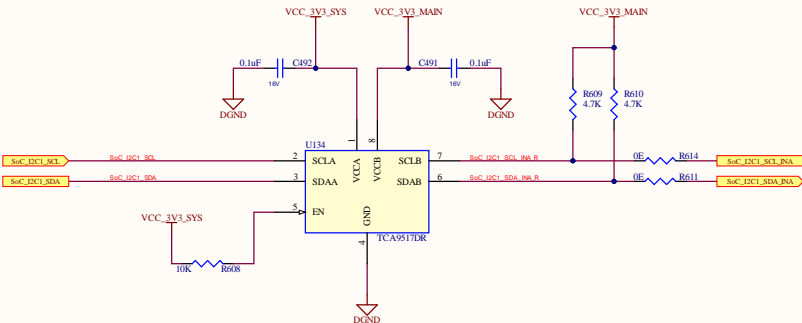
SoC_I2C1_SCL ~~TP14~~
SoC_I2C1_SDA ~~TP12~~
Silk: SOC_I2C1

CURRENT MONITORING DEVICES - 1_A

CAD Note :Follow Kelvin current sense routing while using 2 terminal resistors



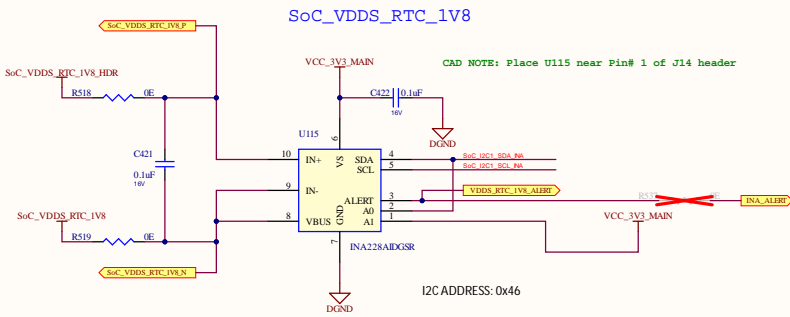
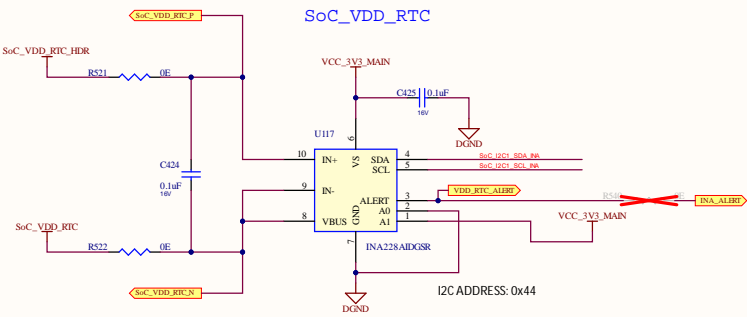
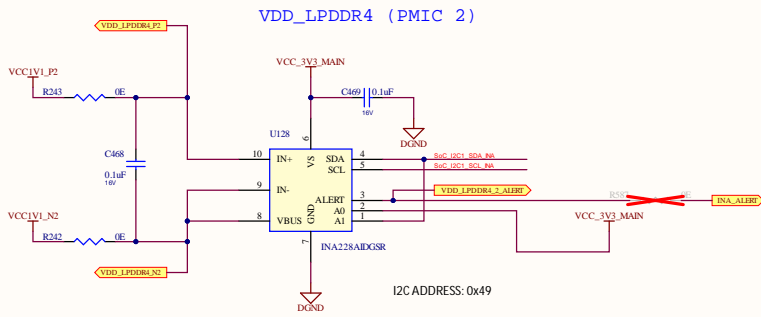
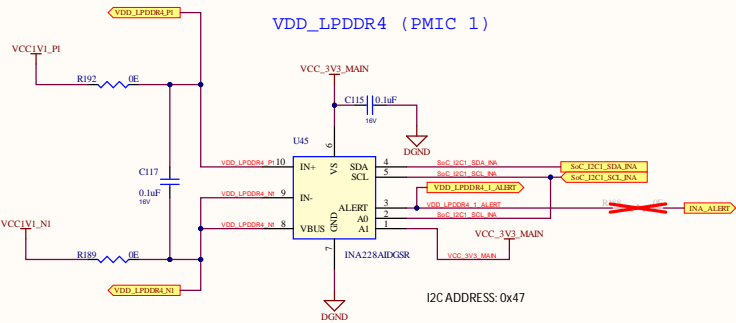
Note:
The design supports current/voltage measurements for the on-board supplies using either INA228 or INA231.
INA228 will be populated on the EVM (Implemented via stacked PCB footprint).



INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (16 HEX)
VCC_CORE	VDD_CORE	40
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC1V8_SYS	SoC_DVDD1V8	45
VEDA1V8	VEDA_1V8	4D
VCC1V1_PMIC1 (from PMIC 1)	VDD_LPDGR4 (from PMIC 1)	47
VCC1V1_PMIC2 (from PMIC 2)	VDD_LPDGR4 (from PMIC 2)	49
SoC_VDD_RTC_HDR	SoC_VDD_RTC	44
SoC_VDD_RTC_1V8_HDR	SoC_VDD_RTC_1V8	46

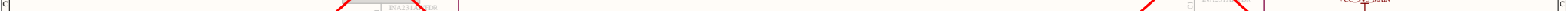
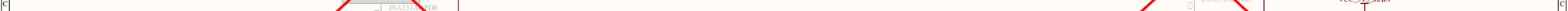
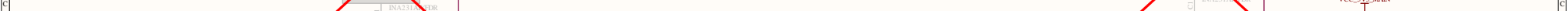
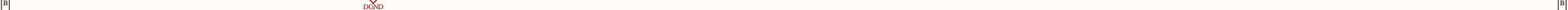
CURRENT MONITORING DEVICES - 1_B

CAD Note : Follow Kelvin current sense routing while using 2 terminal resistors



Note:
The design supports current/voltage measurements for the on-board supplies using either INA228 or INA231.
INA228 will be populated on the EVM (Implemented via stacked PCB footprint).

INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (16 HEX)
VCC_CORE	VDD_CORE	40
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC1V8_SYS	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V1_PMIC1 (From PMIC 1)	VDD_LPDDR4 (From PMIC 1)	47
VCC1V1_PMIC2 (From PMIC 2)	VDD_LPDDR4 (From PMIC 2)	49
SoC_VDD_RTC_HDR	SoC_VDD_RTC	44
SoC_VDD_RTC_1V8_HDR	SoC_VDD_RTC_1V8	46



TNA228 will be populated on the EVM (Implemented via stacked PCB footprint).

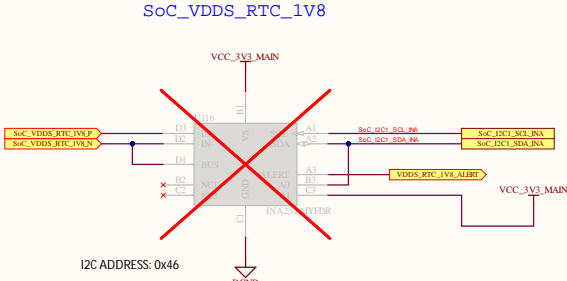
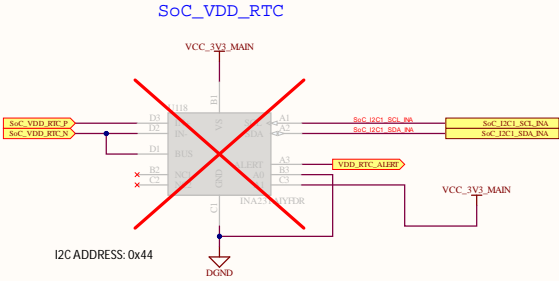
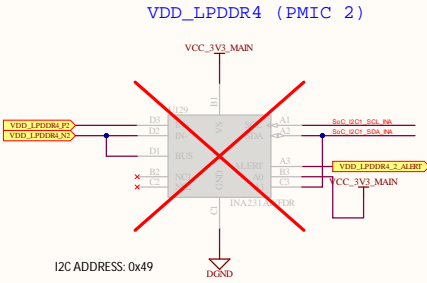
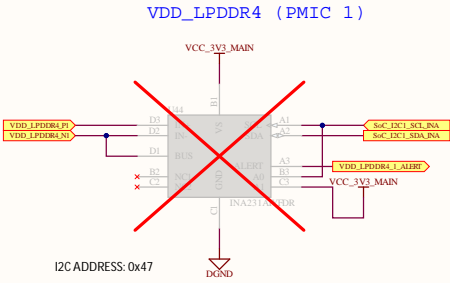
TNA228 will be populated on the EVM (Implemented via stacked PCB footprint).

TNA228 will be populated on the EVM (Implemented via stacked PCB footprint).

1997		
2000	0.10.2000	1.00.2000

1997		
2000	0.10.2000	1.00.2000

CURRENT MONITORING DEVICES - 2_B



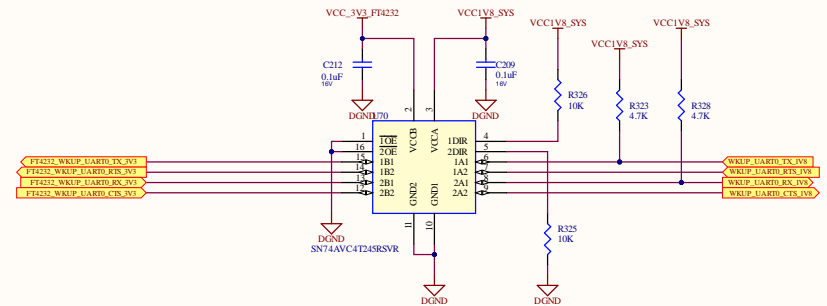
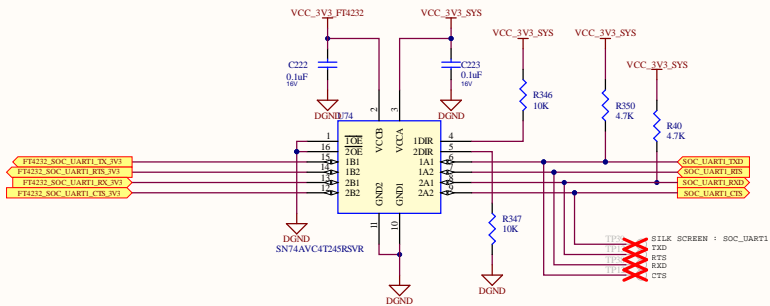
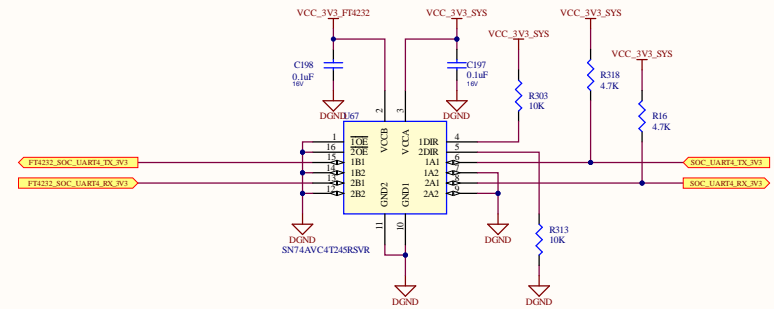
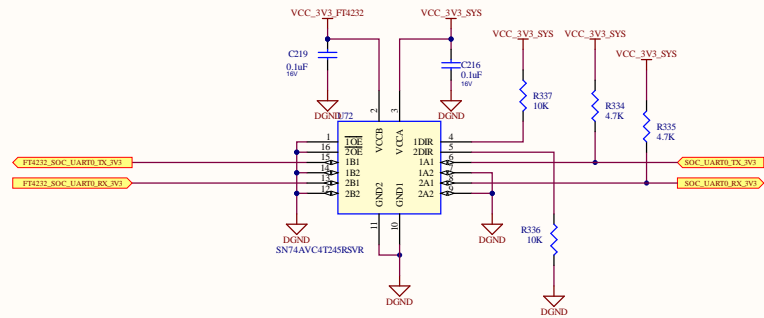
Note:
The design supports current/voltage measurements for the on-board supplies using either INA228 or INA231.
INA228 will be populated on the EVM (Implemented via stacked PCB footprint).

INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_3V3_SYS	SoC_VDD3V3	4C
VCC1V8_SYS	SoC_VDD1V8	45
VDD1V8	VDDA_1V8	4D
VCC1V1_PMIC1 (from PMIC 1)	VDD_LPDDR4 (from PMIC 1)	47
VCC1V1_PMIC2 (from PMIC 2)	VDD_LPDDR4 (from PMIC 2)	49
SoC_VDD_RTC_HDR	SoC_VDD_RTC	44
SoC_VDDS_RTC_1V8_HDR	SoC_VDDS_RTC_1V8	46

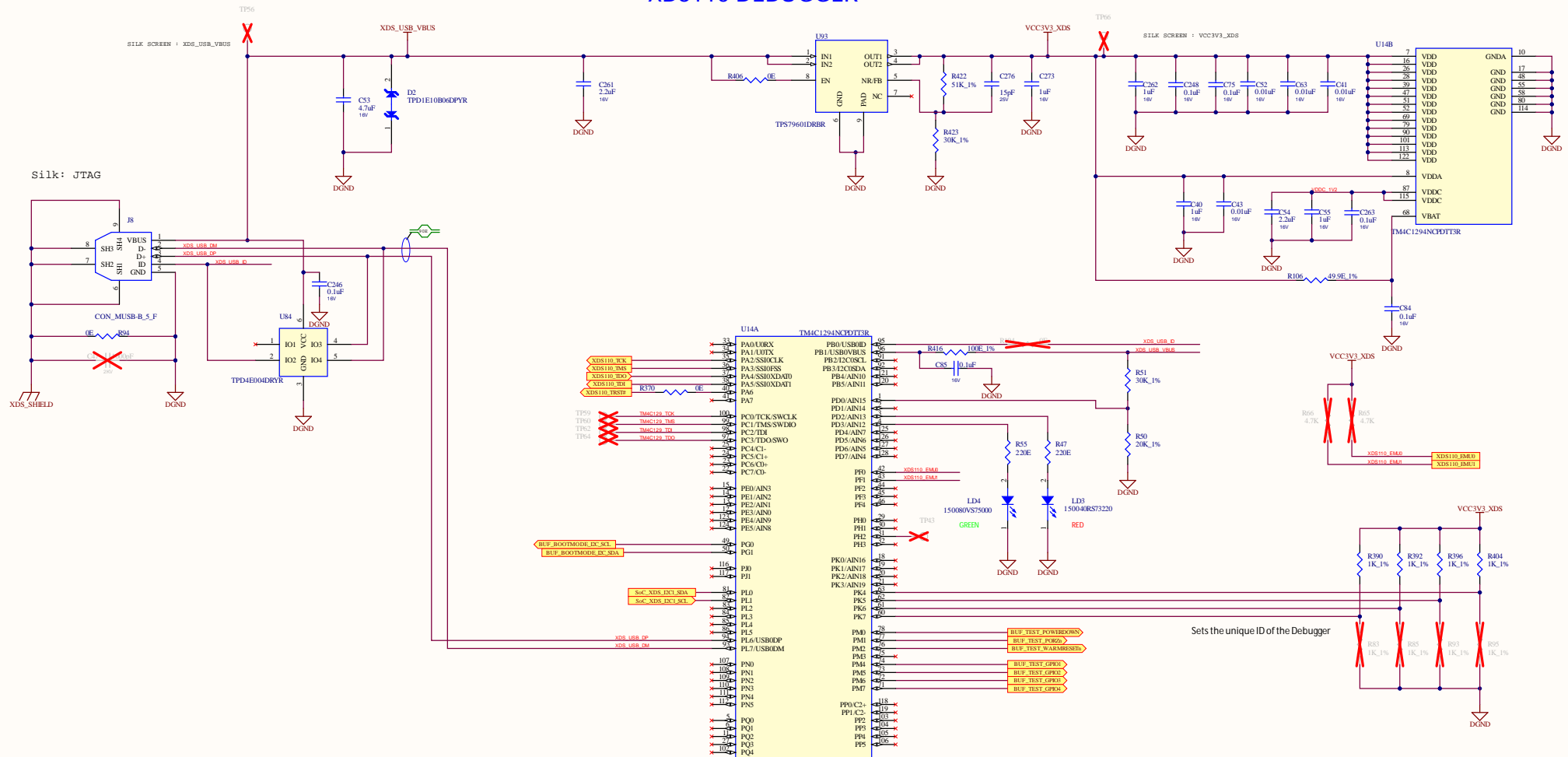
USB TO UART BRIDGE



FT4232 UART BUFFERS

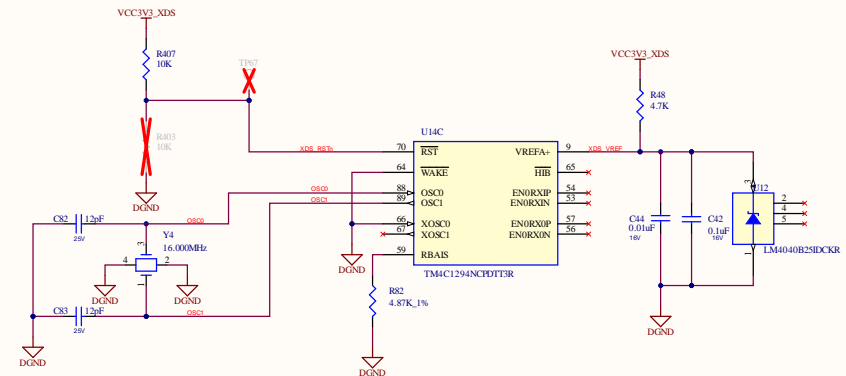


XDS110 DEBUGGER



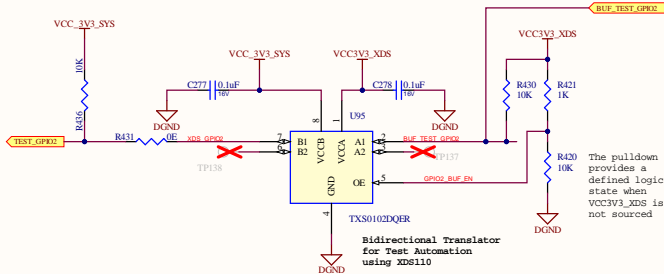
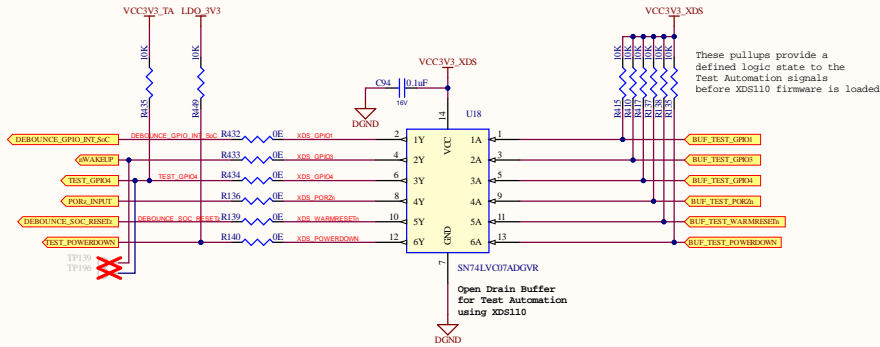
TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on GPIO0_90 Pin of SoC	OUTPUT	External Pullup
TEST_GPIO2	Connected to IO Expander to Communicate with SOC	OUTPUT	External Pullup
TEST_GPIO3	Used as nWAKEUP signal of SoC	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup

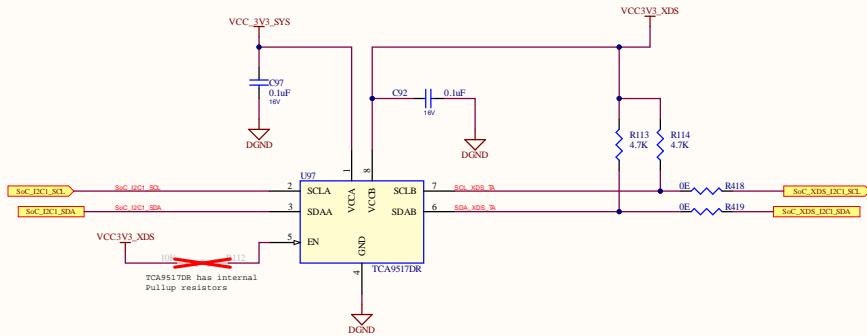


Title			
Size	Number	Revision	
A4	PROC181E1-1		
Date:	7-10-2025	Sheet of	
File:	D:\Arvind\...54 SchlDoc	Drawn By:	

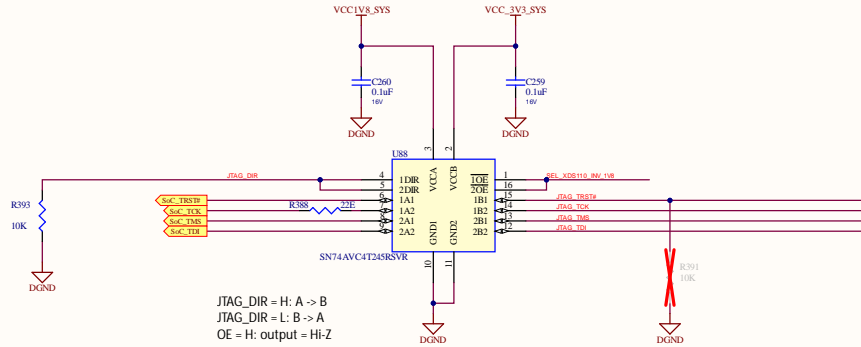
XDS110 TEST AUTOMATION BUFFERS



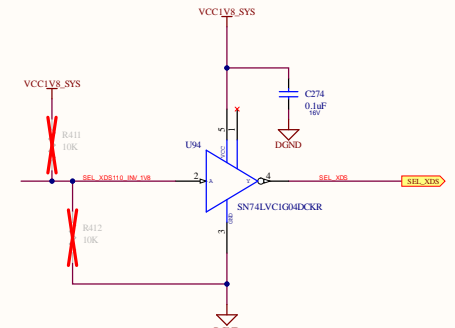
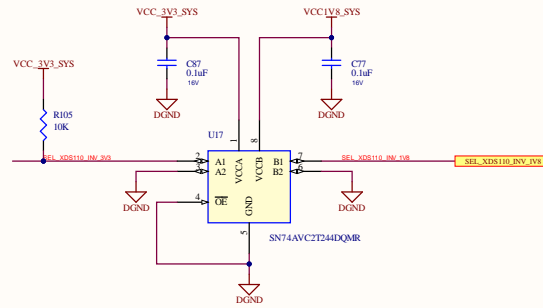
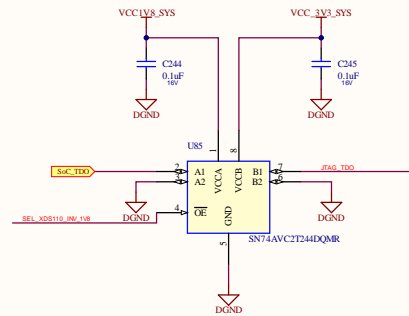
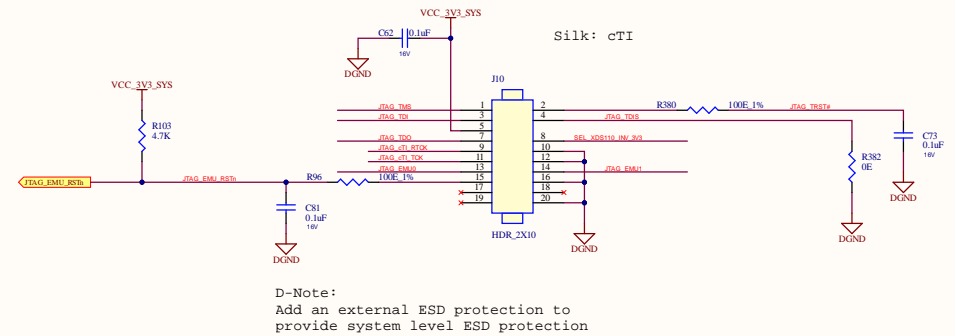
SOC I2C BUS BUFFER



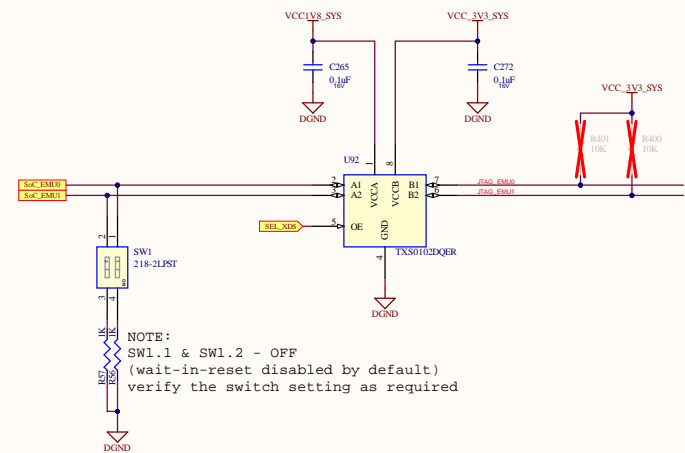
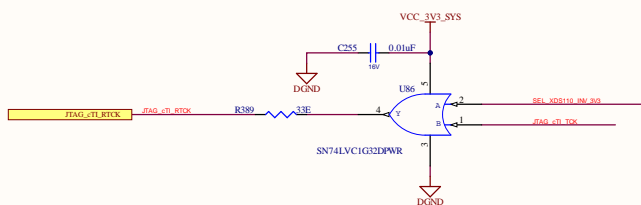
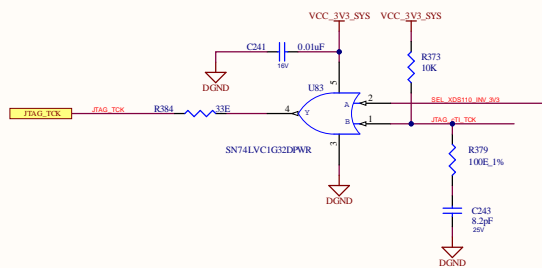
JTAG2 BUFFERS



cTI20 JTAG CONNECTOR



JTAG2 CLOCK BUFFER



Title		
Size	Number	Revision
A4	PROC181E1-1	
Date:	7-10-2025	Sheet of
File:	D:\Arvind\..._56SchDoc	Drawn By:

MOUNTING HARDWARE

ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

BARE PCB



LOGOs



AM62L SOCKET



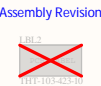
JUMPERS



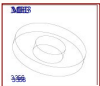
FIDUCIALS



LABELS



SCREW & WASHER FOR PCIe M.2



HOUSING & CRIMP FOR DSI HEADER

